

Sitronix

ST7637

65K 132x132 Color Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7637 is a driver & controller LSI for 65K color graphic dot-matrix liquid crystal display systems. It generates 396 Segment and 132 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit/16-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver Output Circuits

- ◆ 396 segment outputs / 132 common outputs

Applicable Duty Ratios

- ◆ Various partial display
- ◆ Partial window moving & data scrolling

Gray-Scale Display

- ◆ 4FRC & 31 PWM function circuit to display 64 gray-scale display
- ◆ Support 8 color mode (Idle mode)

On-chip Display Data RAM

- ◆ Capacity: 132 x 132 x 16 =278,784 bits

Color support by Interface

- ◆ 256 colors (RGB)=(332) mode
- ◆ 4k colors (RGB)=(444) mode
- ◆ 65K colors (RGB)=(565) mode
- ◆ Truncated 262K colors (RGB)=(666) mode
- ◆ Truncated 16M colors (RGB)=(888) mode

Microprocessor Interface

- ◆ 8/16-bit parallel bi-directional interface with 6800-series or 8080-series
- ◆ 4-line serial interface

- ◆ 3-line (9-bits) serial interface

On-chip Low Power Analog Circuit

- ◆ On-chip oscillator circuit
- ◆ Voltage converter (x2~x8) with internal capacitors.
- ◆ Extremely Few Outsider Components. (3 Capacitors)
- ◆ On-chip Voltage Regulator
- ◆ On-chip electronic contrast control function
- ◆ Voltage follower (LCD bias: 1/5~1/12)

Operating Voltage Range

- ◆ Supply Digital Voltage (VDD, VDD1): 1.65 to 3.0V
- ◆ Supply Analog Voltage (VDD2~VDD5): 2.4 to 3.3V
- ◆ LCD driving voltage (VOP = V0 - VSS): Max: 18V

LCD Driving Voltage (OTP)

- ◆ Contrast Adjustment Value is stored in the Built-In OTP-ROM for better display quality.

LCD Driving setting suggestion

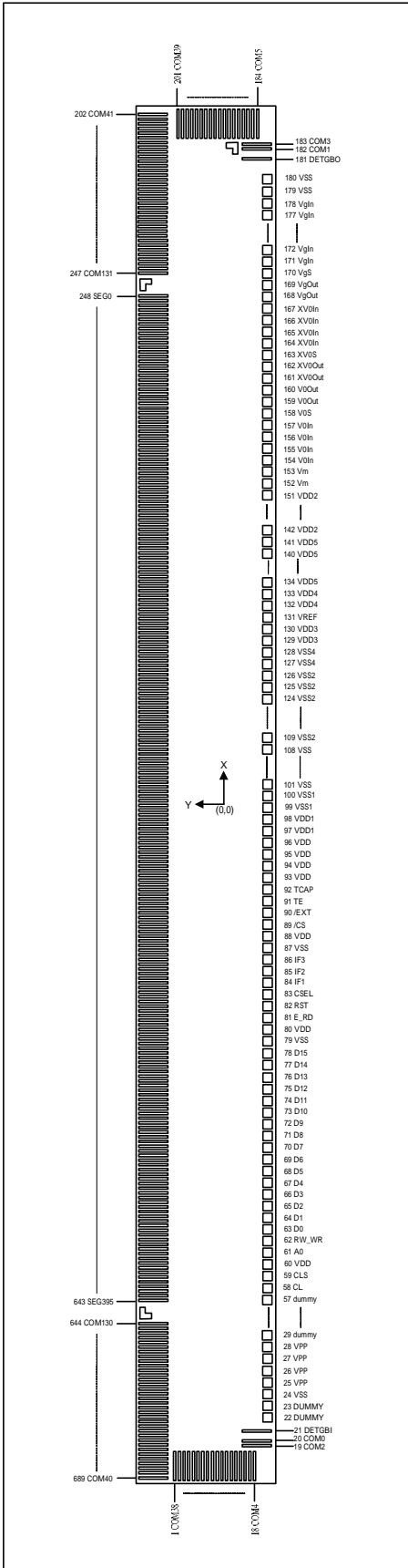
- ◆ VOP = 14V, BIAS=1/9. (VDD=2.8V)
- ◆ VOP=15.5V, BIAS=1/10. (VDD=2.8V)

Package Type

- ◆ Application for COG

ST7637	6800, 8080, 4-Line, 3-Line interface	
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3. ST7637 Pad Arrangement (COG)



Chip Size :

13600 um x 840 um

Bump Pitch :

PAD 1~ 18, 19~20, 182~183, 184~201, 202~247,

pitch=27um (min, com/seg)

PAD 248~643, 644~689 pitch=27um (min, com/seg)

PAD 22 ~ 28,29~180 pitch=80um (I/O)

PAD 20~21, 181~182 pitch=60.15um

PAD 28 ~ 29 pitch=126.53um (I/O)

Bump Size :

PAD 1 ~ 21, PAD 181 ~ 689

Bump width=14um (min, com/seg)

Bump space=13um(min, com/seg)

Bump length=128.58um(min, com/seg)

Bump area=1800um²(com/seg)

PAD 22~180

Bump width=65um(I/O)

Bump space=15um(I/O)

Bump length=63um(I/O)

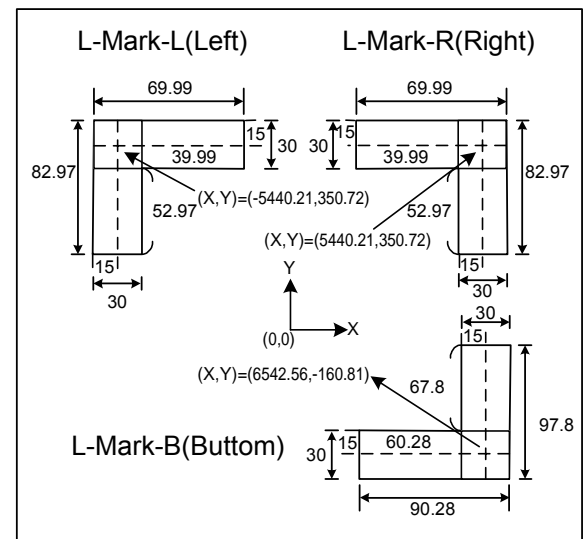
Bump area=4095um²

Bump Height : 15 um

Chip Thickness : 400 um

Alignment mark

The center of alignment mark: see bellow Table



4. Pad Center Coordinates

PAD	NAME	X	Y
1	COM38	-6682.71	146.94
2	COM36	-6682.71	119.94
3	COM34	-6682.71	92.94
4	COM32	-6682.71	65.94
5	COM30	-6682.71	38.94
6	COM28	-6682.71	11.94
7	COM26	-6682.71	-15.06
8	COM24	-6682.71	-42.06
9	COM22	-6682.71	-69.06
10	COM20	-6682.71	-96.06
11	COM18	-6682.71	-123.06
12	COM16	-6682.71	-150.06
13	COM14	-6682.71	-177.06
14	COM12	-6682.71	-204.06
15	COM10	-6682.71	-231.06
16	COM8	-6682.71	-258.06
17	COM6	-6682.71	-285.06
18	COM4	-6682.71	-312.06
19	COM2	-6534.45	-302.71
20	COM0	-6507.45	-302.71
21	DETGBI	-6447.3	-302.71
22	DUMMY	-6370.88	-329.5
23	DUMMY	-6290.88	-329.5
24	VSS	-6210.88	-329.5
25	VPP	-6130.88	-329.5
26	VPP	-6050.88	-329.5
27	VPP	-5970.88	-329.5
28	VPP	-5890.88	-329.5
29	DUMMY	-5764.35	-329.5
30	DUMMY	-5684.35	-329.5
31	DUMMY	-5604.35	-329.5
32	DUMMY	-5524.35	-329.5
33	DUMMY	-5444.35	-329.5
34	DUMMY	-5364.35	-329.5

35	DUMMY	-5284.35	-329.5
36	DUMMY	-5204.35	-329.5
37	DUMMY	-5124.35	-329.5
38	DUMMY	-5044.35	-329.5
39	DUMMY	-4964.35	-329.5
40	DUMMY	-4884.35	-329.5
41	DUMMY	-4804.35	-329.5
42	DUMMY	-4724.35	-329.5
43	DUMMY	-4644.35	-329.5
44	DUMMY	-4564.35	-329.5
45	DUMMY	-4484.35	-329.5
46	DUMMY	-4404.35	-329.5
47	DUMMY	-4324.35	-329.5
48	DUMMY	-4244.35	-329.5
49	DUMMY	-4164.35	-329.5
50	DUMMY	-4084.35	-329.5
51	DUMMY	-4004.35	-329.5
52	DUMMY	-3924.35	-329.5
53	DUMMY	-3844.35	-329.5
54	DUMMY	-3764.35	-329.5
55	DUMMY	-3684.35	-329.5
56	DUMMY	-3604.35	-329.5
57	DUMMY	-3524.35	-329.5
58	CL	-3444.35	-329.5
59	CLS	-3364.35	-329.5
60	VDD	-3284.35	-329.5
61	A0	-3204.35	-329.5
62	RW_WR	-3124.35	-329.5
63	D0	-3044.35	-329.5
64	D1	-2964.35	-329.5
65	D2	-2884.35	-329.5
66	D3	-2804.35	-329.5
67	D4	-2724.35	-329.5
68	D5	-2644.35	-329.5
69	D6	-2564.35	-329.5
70	D7	-2484.35	-329.5

ST7637

71	D8	-2404.35	-329.5
72	D9	-2324.35	-329.5
73	D10	-2244.35	-329.5
74	D11	-2164.35	-329.5
75	D12	-2084.35	-329.5
76	D13	-2004.35	-329.5
77	D14	-1924.35	-329.5
78	D15	-1844.35	-329.5
79	VSS	-1764.35	-329.5
80	VDD	-1684.35	-329.5
81	E_RD	-1604.35	-329.5
82	/RST	-1524.35	-329.5
83	CSEL	-1444.35	-329.5
84	IF1	-1364.35	-329.5
85	IF2	-1284.35	-329.5
86	IF3	-1204.35	-329.5
87	VSS	-1124.35	-329.5
88	VDD	-1044.35	-329.5
89	/CS	-964.35	-329.5
90	/EXT	-884.35	-329.5
91	TE	-804.35	-329.5
92	TCAP	-724.35	-329.5
93	VDD	-644.35	-329.5
94	VDD	-564.35	-329.5
95	VDD	-484.35	-329.5
96	VDD	-404.35	-329.5
97	VDD1	-324.35	-329.5
98	VDD1	-244.35	-329.5
99	VSS1	-164.35	-329.5
100	VSS1	-84.35	-329.5
101	VSS	-4.35	-329.5
102	VSS	75.65	-329.5
103	VSS	155.65	-329.5
104	VSS	235.65	-329.5
105	VSS	315.65	-329.5
106	VSS	395.65	-329.5
107	VSS	475.65	-329.5

108	VSS	555.65	-329.5
109	VSS2	635.65	-329.5
110	VSS2	715.65	-329.5
111	VSS2	795.65	-329.5
112	VSS2	875.65	-329.5
113	VSS2	955.65	-329.5
114	VSS2	1035.65	-329.5
115	VSS2	1115.65	-329.5
116	VSS2	1195.65	-329.5
117	VSS2	1275.65	-329.5
118	VSS2	1355.65	-329.5
119	VSS2	1435.65	-329.5
120	VSS2	1515.65	-329.5
121	VSS2	1595.65	-329.5
122	VSS2	1675.65	-329.5
123	VSS2	1755.65	-329.5
124	VSS2	1835.65	-329.5
125	VSS2	1915.65	-329.5
126	VSS2	1995.65	-329.5
127	VSS4	2075.65	-329.5
128	VSS4	2155.65	-329.5
129	VDD3	2235.65	-329.5
130	VDD3	2315.65	-329.5
131	VREFP	2395.65	-329.5
132	VDD4	2475.65	-329.5
133	VDD4	2555.65	-329.5
134	VDD5	2635.65	-329.5
135	VDD5	2715.65	-329.5
136	VDD5	2795.65	-329.5
137	VDD5	2875.65	-329.5
138	VDD5	2955.65	-329.5
139	VDD5	3035.65	-329.5
140	VDD5	3115.65	-329.5
141	VDD5	3195.65	-329.5
142	VDD2	3275.65	-329.5
143	VDD2	3355.65	-329.5
144	VDD2	3435.65	-329.5

ST7637

145	VDD2	3515.65	-329.5
146	VDD2	3595.65	-329.5
147	VDD2	3675.65	-329.5
148	VDD2	3755.65	-329.5
149	VDD2	3835.65	-329.5
150	VDD2	3915.65	-329.5
151	VDD2	3995.65	-329.5
152	Vm	4075.65	-329.5
153	Vm	4155.65	-329.5
154	V0in	4235.65	-329.5
155	V0in	4315.65	-329.5
156	V0in	4395.65	-329.5
157	V0in	4475.65	-329.5
158	V0s	4555.65	-329.5
159	V0out	4635.65	-329.5
160	V0out	4715.65	-329.5
161	XV0out	4795.65	-329.5
162	XV0out	4875.65	-329.5
163	XV0s	4955.65	-329.5
164	XV0in	5035.65	-329.5
165	XV0in	5115.65	-329.5
166	XV0in	5195.65	-329.5
167	XV0in	5275.65	-329.5
168	Vgout	5355.65	-329.5
169	Vgout	5435.65	-329.5
170	Vgs	5515.65	-329.5
171	Vgin	5595.65	-329.5
172	Vgin	5675.65	-329.5
173	Vgin	5755.65	-329.5
174	Vgin	5835.65	-329.5
175	Vgin	5915.65	-329.5
176	Vgin	5995.65	-329.5
177	Vgin	6075.65	-329.5
178	Vgin	6155.65	-329.5
179	VSS	6235.65	-329.5
180	VSS	6315.65	-329.5
181	DETGBO	6447.3	-302.71

182	COM1	6507.45	-302.71
183	COM3	6534.45	-302.71
184	COM5	6682.71	-312.06
185	COM7	6682.71	-285.06
186	COM9	6682.71	-258.06
187	COM11	6682.71	-231.06
188	COM13	6682.71	-204.06
189	COM15	6682.71	-177.06
190	COM17	6682.71	-150.06
191	COM19	6682.71	-123.06
192	COM21	6682.71	-96.06
193	COM23	6682.71	-69.06
194	COM25	6682.71	-42.06
195	COM27	6682.71	-15.06
196	COM29	6682.71	11.94
197	COM31	6682.71	38.94
198	COM33	6682.71	65.94
199	COM35	6682.71	92.94
200	COM37	6682.71	119.94
201	COM39	6682.71	146.94
202	COM41	6706.5	302.71
203	COM43	6679.5	302.71
204	COM45	6652.5	302.71
205	COM47	6625.5	302.71
206	COM49	6598.5	302.71
207	COM51	6571.5	302.71
208	COM53	6544.5	302.71
209	COM55	6517.5	302.71
210	COM57	6490.5	302.71
211	COM59	6463.5	302.71
212	COM61	6436.5	302.71
213	COM63	6409.5	302.71
214	COM65	6382.5	302.71
215	COM67	6355.5	302.71
216	COM69	6328.5	302.71
217	COM71	6301.5	302.71
218	COM73	6274.5	302.71

ST7637

219	COM75	6247.5	302.71
220	COM77	6220.5	302.71
221	COM79	6193.5	302.71
222	COM81	6166.5	302.71
223	COM83	6139.5	302.71
224	COM85	6112.5	302.71
225	COM87	6085.5	302.71
226	COM89	6058.5	302.71
227	COM91	6031.5	302.71
228	COM93	6004.5	302.71
229	COM95	5977.5	302.71
230	COM97	5950.5	302.71
231	COM99	5923.5	302.71
232	COM101	5896.5	302.71
233	COM103	5869.5	302.71
234	COM105	5842.5	302.71
235	COM107	5815.5	302.71
236	COM109	5788.5	302.71
237	COM111	5761.5	302.71
238	COM113	5734.5	302.71
239	COM115	5707.5	302.71
240	COM117	5680.5	302.71
241	COM119	5653.5	302.71
242	COM121	5626.5	302.71
243	COM123	5599.5	302.71
244	COM125	5572.5	302.71
245	COM127	5545.5	302.71
246	COM129	5518.5	302.71
247	COM131	5491.5	302.71
248	SEG0	5332.5	302.71
249	SEG1	5305.5	302.71
250	SEG2	5278.5	302.71
251	SEG3	5251.5	302.71
252	SEG4	5224.5	302.71
253	SEG5	5197.5	302.71
254	SEG6	5170.5	302.71
255	SEG7	5143.5	302.71

256	SEG8	5116.5	302.71
257	SEG9	5089.5	302.71
258	SEG10	5062.5	302.71
259	SEG11	5035.5	302.71
260	SEG12	5008.5	302.71
261	SEG13	4981.5	302.71
262	SEG14	4954.5	302.71
263	SEG15	4927.5	302.71
264	SEG16	4900.5	302.71
265	SEG17	4873.5	302.71
266	SEG18	4846.5	302.71
267	SEG19	4819.5	302.71
268	SEG20	4792.5	302.71
269	SEG21	4765.5	302.71
270	SEG22	4738.5	302.71
271	SEG23	4711.5	302.71
272	SEG24	4684.5	302.71
273	SEG25	4657.5	302.71
274	SEG26	4630.5	302.71
275	SEG27	4603.5	302.71
276	SEG28	4576.5	302.71
277	SEG29	4549.5	302.71
278	SEG30	4522.5	302.71
279	SEG31	4495.5	302.71
280	SEG32	4468.5	302.71
281	SEG33	4441.5	302.71
282	SEG34	4414.5	302.71
283	SEG35	4387.5	302.71
284	SEG36	4360.5	302.71
285	SEG37	4333.5	302.71
286	SEG38	4306.5	302.71
287	SEG39	4279.5	302.71
288	SEG40	4252.5	302.71
289	SEG41	4225.5	302.71
290	SEG42	4198.5	302.71
291	SEG43	4171.5	302.71
292	SEG44	4144.5	302.71

ST7637

293	SEG45	4117.5	302.71
294	SEG46	4090.5	302.71
295	SEG47	4063.5	302.71
296	SEG48	4036.5	302.71
297	SEG49	4009.5	302.71
298	SEG50	3982.5	302.71
299	SEG51	3955.5	302.71
300	SEG52	3928.5	302.71
301	SEG53	3901.5	302.71
302	SEG54	3874.5	302.71
303	SEG55	3847.5	302.71
304	SEG56	3820.5	302.71
305	SEG57	3793.5	302.71
306	SEG58	3766.5	302.71
307	SEG59	3739.5	302.71
308	SEG60	3712.5	302.71
309	SEG61	3685.5	302.71
310	SEG62	3658.5	302.71
311	SEG63	3631.5	302.71
312	SEG64	3604.5	302.71
313	SEG65	3577.5	302.71
314	SEG66	3550.5	302.71
315	SEG67	3523.5	302.71
316	SEG68	3496.5	302.71
317	SEG69	3469.5	302.71
318	SEG70	3442.5	302.71
319	SEG71	3415.5	302.71
320	SEG72	3388.5	302.71
321	SEG73	3361.5	302.71
322	SEG74	3334.5	302.71
323	SEG75	3307.5	302.71
324	SEG76	3280.5	302.71
325	SEG77	3253.5	302.71
326	SEG78	3226.5	302.71
327	SEG79	3199.5	302.71
328	SEG80	3172.5	302.71
329	SEG81	3145.5	302.71

330	SEG82	3118.5	302.71
331	SEG83	3091.5	302.71
332	SEG84	3064.5	302.71
333	SEG85	3037.5	302.71
334	SEG86	3010.5	302.71
335	SEG87	2983.5	302.71
336	SEG88	2956.5	302.71
337	SEG89	2929.5	302.71
338	SEG90	2902.5	302.71
339	SEG91	2875.5	302.71
340	SEG92	2848.5	302.71
341	SEG93	2821.5	302.71
342	SEG94	2794.5	302.71
343	SEG95	2767.5	302.71
344	SEG96	2740.5	302.71
345	SEG97	2713.5	302.71
346	SEG98	2686.5	302.71
347	SEG99	2659.5	302.71
348	SEG100	2632.5	302.71
349	SEG101	2605.5	302.71
350	SEG102	2578.5	302.71
351	SEG103	2551.5	302.71
352	SEG104	2524.5	302.71
353	SEG105	2497.5	302.71
354	SEG106	2470.5	302.71
355	SEG107	2443.5	302.71
356	SEG108	2416.5	302.71
357	SEG109	2389.5	302.71
358	SEG110	2362.5	302.71
359	SEG111	2335.5	302.71
360	SEG112	2308.5	302.71
361	SEG113	2281.5	302.71
362	SEG114	2254.5	302.71
363	SEG115	2227.5	302.71
364	SEG116	2200.5	302.71
365	SEG117	2173.5	302.71
366	SEG118	2146.5	302.71

ST7637

367	SEG119	2119.5	302.71
368	SEG120	2092.5	302.71
369	SEG121	2065.5	302.71
370	SEG122	2038.5	302.71
371	SEG123	2011.5	302.71
372	SEG124	1984.5	302.71
373	SEG125	1957.5	302.71
374	SEG126	1930.5	302.71
375	SEG127	1903.5	302.71
376	SEG128	1876.5	302.71
377	SEG129	1849.5	302.71
378	SEG130	1822.5	302.71
379	SEG131	1795.5	302.71
380	SEG132	1768.5	302.71
381	SEG133	1741.5	302.71
382	SEG134	1714.5	302.71
383	SEG135	1687.5	302.71
384	SEG136	1660.5	302.71
385	SEG137	1633.5	302.71
386	SEG138	1606.5	302.71
387	SEG139	1579.5	302.71
388	SEG140	1552.5	302.71
389	SEG141	1525.5	302.71
390	SEG142	1498.5	302.71
391	SEG143	1471.5	302.71
392	SEG144	1444.5	302.71
393	SEG145	1417.5	302.71
394	SEG146	1390.5	302.71
395	SEG147	1363.5	302.71
396	SEG148	1336.5	302.71
397	SEG149	1309.5	302.71
398	SEG150	1282.5	302.71
399	SEG151	1255.5	302.71
400	SEG152	1228.5	302.71
401	SEG153	1201.5	302.71
402	SEG154	1174.5	302.71
403	SEG155	1147.5	302.71

404	SEG156	1120.5	302.71
405	SEG157	1093.5	302.71
406	SEG158	1066.5	302.71
407	SEG159	1039.5	302.71
408	SEG160	1012.5	302.71
409	SEG161	985.5	302.71
410	SEG162	958.5	302.71
411	SEG163	931.5	302.71
412	SEG164	904.5	302.71
413	SEG165	877.5	302.71
414	SEG166	850.5	302.71
415	SEG167	823.5	302.71
416	SEG168	796.5	302.71
417	SEG169	769.5	302.71
418	SEG170	742.5	302.71
419	SEG171	715.5	302.71
420	SEG172	688.5	302.71
421	SEG173	661.5	302.71
422	SEG174	634.5	302.71
423	SEG175	607.5	302.71
424	SEG176	580.5	302.71
425	SEG177	553.5	302.71
426	SEG178	526.5	302.71
427	SEG179	499.5	302.71
428	SEG180	472.5	302.71
429	SEG181	445.5	302.71
430	SEG182	418.5	302.71
431	SEG183	391.5	302.71
432	SEG184	364.5	302.71
433	SEG185	337.5	302.71
434	SEG186	310.5	302.71
435	SEG187	283.5	302.71
436	SEG188	256.5	302.71
437	SEG189	229.5	302.71
438	SEG190	202.5	302.71
439	SEG191	175.5	302.71
440	SEG192	148.5	302.71

ST7637

441	SEG193	121.5	302.71
442	SEG194	94.5	302.71
443	SEG195	67.5	302.71
444	SEG196	40.5	302.71
445	SEG197	13.5	302.71
446	SEG198	-13.5	302.71
447	SEG199	-40.5	302.71
448	SEG200	-67.5	302.71
449	SEG201	-94.5	302.71
450	SEG202	-121.5	302.71
451	SEG203	-148.5	302.71
452	SEG204	-175.5	302.71
453	SEG205	-202.5	302.71
454	SEG206	-229.5	302.71
455	SEG207	-256.5	302.71
456	SEG208	-283.5	302.71
457	SEG209	-310.5	302.71
458	SEG210	-337.5	302.71
459	SEG211	-364.5	302.71
460	SEG212	-391.5	302.71
461	SEG213	-418.5	302.71
462	SEG214	-445.5	302.71
463	SEG215	-472.5	302.71
464	SEG216	-499.5	302.71
465	SEG217	-526.5	302.71
466	SEG218	-553.5	302.71
467	SEG219	-580.5	302.71
468	SEG220	-607.5	302.71
469	SEG221	-634.5	302.71
470	SEG222	-661.5	302.71
471	SEG223	-688.5	302.71
472	SEG224	-715.5	302.71
473	SEG225	-742.5	302.71
474	SEG226	-769.5	302.71
475	SEG227	-796.5	302.71
476	SEG228	-823.5	302.71
477	SEG229	-850.5	302.71

478	SEG230	-877.5	302.71
479	SEG231	-904.5	302.71
480	SEG232	-931.5	302.71
481	SEG233	-958.5	302.71
482	SEG234	-985.5	302.71
483	SEG235	-1012.5	302.71
484	SEG236	-1039.5	302.71
485	SEG237	-1066.5	302.71
486	SEG238	-1093.5	302.71
487	SEG239	-1120.5	302.71
488	SEG240	-1147.5	302.71
489	SEG241	-1174.5	302.71
490	SEG242	-1201.5	302.71
491	SEG243	-1228.5	302.71
492	SEG244	-1255.5	302.71
493	SEG245	-1282.5	302.71
494	SEG246	-1309.5	302.71
495	SEG247	-1336.5	302.71
496	SEG248	-1363.5	302.71
497	SEG249	-1390.5	302.71
498	SEG250	-1417.5	302.71
499	SEG251	-1444.5	302.71
500	SEG252	-1471.5	302.71
501	SEG253	-1498.5	302.71
502	SEG254	-1525.5	302.71
503	SEG255	-1552.5	302.71
504	SEG256	-1579.5	302.71
505	SEG257	-1606.5	302.71
506	SEG258	-1633.5	302.71
507	SEG259	-1660.5	302.71
508	SEG260	-1687.5	302.71
509	SEG261	-1714.5	302.71
510	SEG262	-1741.5	302.71
511	SEG263	-1768.5	302.71
512	SEG264	-1795.5	302.71
513	SEG265	-1822.5	302.71
514	SEG266	-1849.5	302.71

ST7637

515	SEG267	-1876.5	302.71
516	SEG268	-1903.5	302.71
517	SEG269	-1930.5	302.71
518	SEG270	-1957.5	302.71
519	SEG271	-1984.5	302.71
520	SEG272	-2011.5	302.71
521	SEG273	-2038.5	302.71
522	SEG274	-2065.5	302.71
523	SEG275	-2092.5	302.71
524	SEG276	-2119.5	302.71
525	SEG277	-2146.5	302.71
526	SEG278	-2173.5	302.71
527	SEG279	-2200.5	302.71
528	SEG280	-2227.5	302.71
529	SEG281	-2254.5	302.71
530	SEG282	-2281.5	302.71
531	SEG283	-2308.5	302.71
532	SEG284	-2335.5	302.71
533	SEG285	-2362.5	302.71
534	SEG286	-2389.5	302.71
535	SEG287	-2416.5	302.71
536	SEG288	-2443.5	302.71
537	SEG289	-2470.5	302.71
538	SEG290	-2497.5	302.71
539	SEG291	-2524.5	302.71
540	SEG292	-2551.5	302.71
541	SEG293	-2578.5	302.71
542	SEG294	-2605.5	302.71
543	SEG295	-2632.5	302.71
544	SEG296	-2659.5	302.71
545	SEG297	-2686.5	302.71
546	SEG298	-2713.5	302.71
547	SEG299	-2740.5	302.71
548	SEG300	-2767.5	302.71
549	SEG301	-2794.5	302.71
550	SEG302	-2821.5	302.71
551	SEG303	-2848.5	302.71

552	SEG304	-2875.5	302.71
553	SEG305	-2902.5	302.71
554	SEG306	-2929.5	302.71
555	SEG307	-2956.5	302.71
556	SEG308	-2983.5	302.71
557	SEG309	-3010.5	302.71
558	SEG310	-3037.5	302.71
559	SEG311	-3064.5	302.71
560	SEG312	-3091.5	302.71
561	SEG313	-3118.5	302.71
562	SEG314	-3145.5	302.71
563	SEG315	-3172.5	302.71
564	SEG316	-3199.5	302.71
565	SEG317	-3226.5	302.71
566	SEG318	-3253.5	302.71
567	SEG319	-3280.5	302.71
568	SEG320	-3307.5	302.71
569	SEG321	-3334.5	302.71
570	SEG322	-3361.5	302.71
571	SEG323	-3388.5	302.71
572	SEG324	-3415.5	302.71
573	SEG325	-3442.5	302.71
574	SEG326	-3469.5	302.71
575	SEG327	-3496.5	302.71
576	SEG328	-3523.5	302.71
577	SEG329	-3550.5	302.71
578	SEG330	-3577.5	302.71
579	SEG331	-3604.5	302.71
580	SEG332	-3631.5	302.71
581	SEG333	-3658.5	302.71
582	SEG334	-3685.5	302.71
583	SEG335	-3712.5	302.71
584	SEG336	-3739.5	302.71
585	SEG337	-3766.5	302.71
586	SEG338	-3793.5	302.71
587	SEG339	-3820.5	302.71
588	SEG340	-3847.5	302.71

ST7637

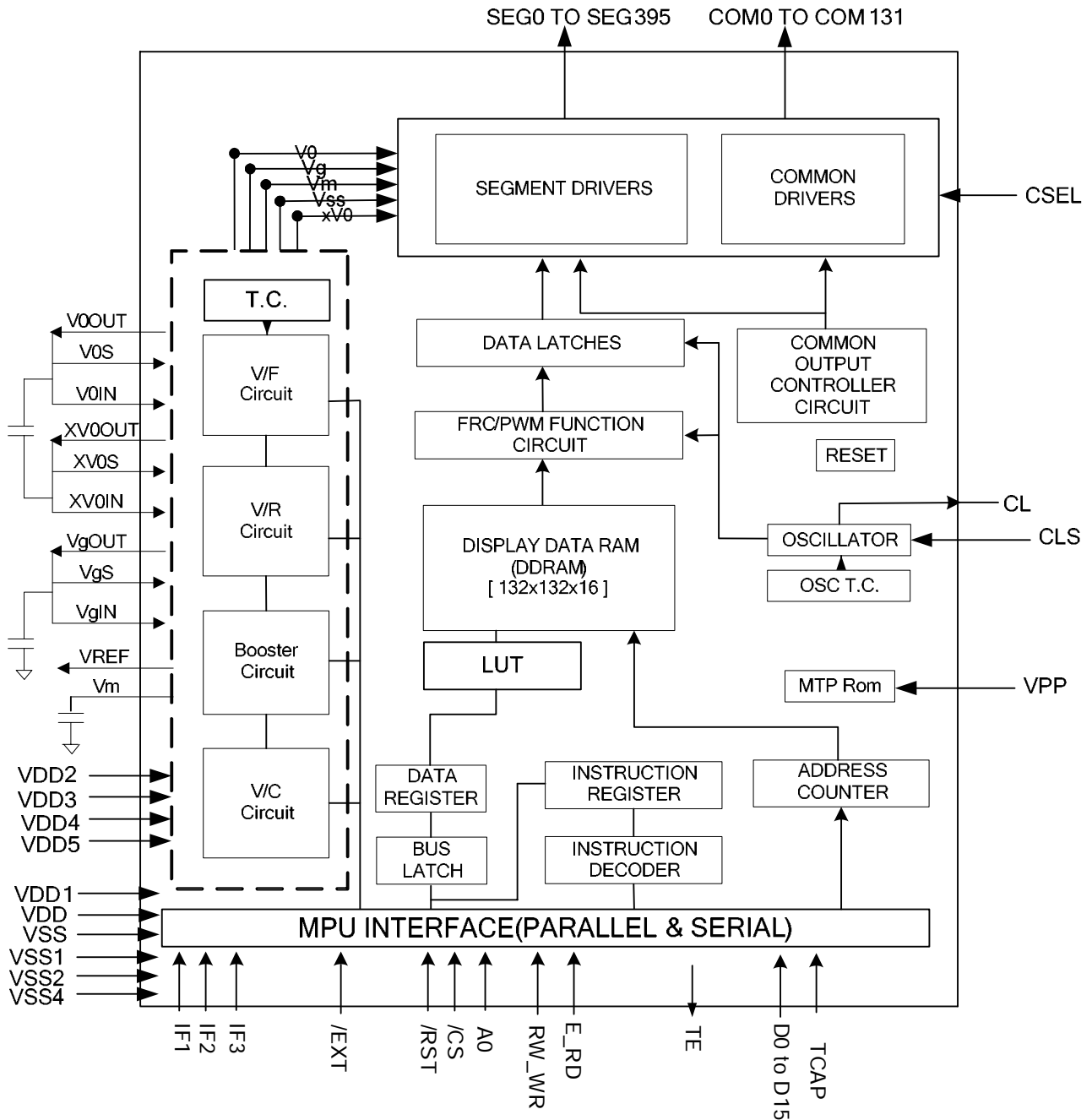
589	SEG341	-3874.5	302.71
590	SEG342	-3901.5	302.71
591	SEG343	-3928.5	302.71
592	SEG344	-3955.5	302.71
593	SEG345	-3982.5	302.71
594	SEG346	-4009.5	302.71
595	SEG347	-4036.5	302.71
596	SEG348	-4063.5	302.71
597	SEG349	-4090.5	302.71
598	SEG350	-4117.5	302.71
599	SEG351	-4144.5	302.71
600	SEG352	-4171.5	302.71
601	SEG353	-4198.5	302.71
602	SEG354	-4225.5	302.71
603	SEG355	-4252.5	302.71
604	SEG356	-4279.5	302.71
605	SEG357	-4306.5	302.71
606	SEG358	-4333.5	302.71
607	SEG359	-4360.5	302.71
608	SEG360	-4387.5	302.71
609	SEG361	-4414.5	302.71
610	SEG362	-4441.5	302.71
611	SEG363	-4468.5	302.71
612	SEG364	-4495.5	302.71
613	SEG365	-4522.5	302.71
614	SEG366	-4549.5	302.71
615	SEG367	-4576.5	302.71
616	SEG368	-4603.5	302.71
617	SEG369	-4630.5	302.71
618	SEG370	-4657.5	302.71
619	SEG371	-4684.5	302.71
620	SEG372	-4711.5	302.71
621	SEG373	-4738.5	302.71
622	SEG374	-4765.5	302.71
623	SEG375	-4792.5	302.71
624	SEG376	-4819.5	302.71
625	SEG377	-4846.5	302.71

626	SEG378	-4873.5	302.71
627	SEG379	-4900.5	302.71
628	SEG380	-4927.5	302.71
629	SEG381	-4954.5	302.71
630	SEG382	-4981.5	302.71
631	SEG383	-5008.5	302.71
632	SEG384	-5035.5	302.71
633	SEG385	-5062.5	302.71
634	SEG386	-5089.5	302.71
635	SEG387	-5116.5	302.71
636	SEG388	-5143.5	302.71
637	SEG389	-5170.5	302.71
638	SEG390	-5197.5	302.71
639	SEG391	-5224.5	302.71
640	SEG392	-5251.5	302.71
641	SEG393	-5278.5	302.71
642	SEG394	-5305.5	302.71
643	SEG395	-5332.5	302.71
644	COM130	-5491.5	302.71
645	COM128	-5518.5	302.71
646	COM126	-5545.5	302.71
647	COM124	-5572.5	302.71
648	COM122	-5599.5	302.71
649	COM120	-5626.5	302.71
650	COM118	-5653.5	302.71
651	COM116	-5680.5	302.71
652	COM114	-5707.5	302.71
653	COM112	-5734.5	302.71
654	COM110	-5761.5	302.71
655	COM108	-5788.5	302.71
656	COM106	-5815.5	302.71
657	COM104	-5842.5	302.71
658	COM102	-5869.5	302.71
659	COM100	-5896.5	302.71
660	COM98	-5923.5	302.71
661	COM96	-5950.5	302.71
662	COM94	-5977.5	302.71

ST7637

663	COM92	-6004.5	302.71
664	COM90	-6031.5	302.71
665	COM88	-6058.5	302.71
666	COM86	-6085.5	302.71
667	COM84	-6112.5	302.71
668	COM82	-6139.5	302.71
669	COM80	-6166.5	302.71
670	COM78	-6193.5	302.71
671	COM76	-6220.5	302.71
672	COM74	-6247.5	302.71
673	COM72	-6274.5	302.71
674	COM70	-6301.5	302.71
675	COM68	-6328.5	302.71
676	COM66	-6355.5	302.71
677	COM64	-6382.5	302.71
678	COM62	-6409.5	302.71
679	COM60	-6436.5	302.71
680	COM58	-6463.5	302.71
681	COM56	-6490.5	302.71
682	COM54	-6517.5	302.71
683	COM52	-6544.5	302.71
684	COM50	-6571.5	302.71
685	COM48	-6598.5	302.71
686	COM46	-6625.5	302.71
687	COM44	-6652.5	302.71
688	COM42	-6679.5	302.71
689	COM40	-6706.5	302.71
690	L-Mark-L(Left)	-5440.21	350.72
691	L-Mark-R(Right)	5440.21	350.72
692	L-Mark-B(Bottom)	6542.56	-160.81

5. Block diagram



6. PIN DESCRIPTION

6.1 Power Supply

Name	I/O	Description
VDD	Supply	Power supply for logic circuit.
VDD1	Supply	Power supply for OSC circuit.
VDD2	Supply	Power supply for Booster circuit.
VDD3	Supply	Power supply for LCD.
VDD4	Supply	Power supply for LCD.
VDD5	Supply	Power supply for LCD.
VSS	Supply	Ground for logic circuit. Ground system should be connected together.
VSS1	Supply	Ground for OSC circuit. Ground system should be connected together.
VSS2	Supply	Ground for Booster circuit. Ground system should be connected together.
VSS4	Supply	Ground for LCD. Ground system should be connected together.

6.2 LCD Power Supply Pins

Name	I/O	Description						
V0 _{OUT} V0 _{IN} V0 _S	I/O	<p>Positive LCD driver supply voltages.</p> <p>V0_{OUT} is the output voltage of V0 generated by ST7637.</p> <p>V0_{IN} is the input pin of power supply to generate V0 voltage for LCD.</p> <p>V0_S is the input pin of power supply to sense the V0 voltage.</p> <p>V0_{OUT}、V0_{IN} & V0_S should be connected together by FPC.</p>						
XV0 _{OUT} XV0 _{IN} XV0 _S	I/O	<p>Negative LCD driver supply voltages.</p> <p>XV0_{OUT} is the output voltage of XV0 generated by ST7637.</p> <p>XV0_{IN} is the input pin of power supply to generate XV0 voltage for LCD.</p> <p>XV0_S is the input pin of power supply to sense the XV0 voltage.</p> <p>XV0_{OUT}、XV0_{IN} & XV0_S should be connected together by FPC.</p>						
Vg _{OUT} Vg _{IN} Vg _S Vm	I/O	<p>Bias LCD driver supply voltages.</p> <p>Vg_{OUT} is the output voltage of Vg generated by ST7637.</p> <p>Vg_{IN} is the input pin of power supply to generate Vg voltage for LCD.</p> <p>Vg_S is the input pin of power supply to sense the Vg voltage.</p> <p>Vg_{OUT}、Vg_{IN} & Vg_S should be connected together by FPC.</p> <p>Vm is the I/O pin of LCD bias supply voltage</p> <p>Voltages should have the following relationship;</p> <p>$V0 > Vg > Vm > VSS > XV0$.</p> <p>$VDDA - 0.7V > Vm > 0.7V$.</p> <p>$VddA < 3V:2 \times VDDA \quad Vg < 3V; \quad VddA < 3V:2 \times VDDA \quad Vg > 1.8V$</p> <p>When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>LCD bias</th> <th>Vg</th> <th>Vm</th> </tr> </thead> <tbody> <tr> <td>1/N bias</td> <td>$(2/N) \times V0$</td> <td>$(1/N) \times V0$</td> </tr> </tbody> </table> <p style="text-align: right;">NOTE: N = 5 to 12</p>	LCD bias	Vg	Vm	1/N bias	$(2/N) \times V0$	$(1/N) \times V0$
LCD bias	Vg	Vm						
1/N bias	$(2/N) \times V0$	$(1/N) \times V0$						

6.3 System Control

Name	I/O	Description
CLS	I	When using internal clock oscillator, connect CLS to VDD. When using external clock oscillator, connect CLS to VSS.
CL	I/O	When using internal clock oscillator, it's oscillator output. When using external clock oscillator, it's clock input.
CSEL	I	This PIN should connect to VDD.
TCAP	I/O	Test pin. Left it opens.
VREF	O	Reference voltage output for monitor only. Left it opened.
VPP	I	When writing OTP, it needs external power supply voltage 7.5V~7.75V input to write successfully.

6.4 Microprocessor Interface

Name	I/O	Description																												
/RST	I	Reset input pin When /RST is "L", initialization is executed.																												
IF[3:1]	I	Parallel / Serial data input select input <table border="1" data-bbox="576 922 1150 1272"> <thead> <tr> <th>IF3</th> <th>IF2</th> <th>IF1</th> <th>MPU interface type</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>H</td> <td>80 series 16-bit parallel</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>80 series 8-bit parallel</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>68 series 16-bit parallel</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>68 series 8-bit parallel</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>8-bit serial (4 line)</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>9-bit serial (3 line)</td> </tr> </tbody> </table> <p>Note: Refer to Table 7.2-1 for detail interface connections.</p>	IF3	IF2	IF1	MPU interface type	H	H	H	80 series 16-bit parallel	H	H	L	80 series 8-bit parallel	H	L	H	68 series 16-bit parallel	H	L	L	68 series 8-bit parallel	L	H	H	8-bit serial (4 line)	L	H	L	9-bit serial (3 line)
IF3	IF2	IF1	MPU interface type																											
H	H	H	80 series 16-bit parallel																											
H	H	L	80 series 8-bit parallel																											
H	L	H	68 series 16-bit parallel																											
H	L	L	68 series 8-bit parallel																											
L	H	H	8-bit serial (4 line)																											
L	H	L	9-bit serial (3 line)																											
/CS	I	Chip select input pins Data / Instruction I/O is enabled only when /CS is "L". When chip select is non-active, D0 to D15 become high impedance.																												
A0	I	Register select input pin In parallel interface: A0 = "H": D0 to D15 or SI are display data A0 = "L": D0 to D15 or SI are control Command In 3-line/4-line interface: This pad will be used for SCL function.																												

RW_WR	I	RW_WR pin is only used in parallel interface.		
		MPU type	RW_WR	Description
		6800-series	RW	Read / Write control input pin Write status: RW = "L". Read status: RW = "H".
8080-series	/WR	Write enable clock input pin The data on D0 to D15 are latched at the rising edge of the /WR signal.		
When in the serial interface, connect it to VDD.				
E_RD	I	E_RD pin is only used in parallel interface.		
		MPU Type	E_RD	Description
		6800-series	E	Enable clock pin: Write status: The data on D0 to D15 are latched at the falling edge of the E signal. Read status: The data on D0 to D15 are latched at the rising edge of the E signal.
8080-series	/RD	Read enable clock input pin The data on D0 to D15 are latched at the falling edge of the /WR signal.		
When in the serial interface, connect it to VDD.				
D15 to D0	I/O	<p>They connect to the standard 8-bit or 16 bit MPU bus via the 8/16 –bit bi-directional bus.</p> <p>When the following interface is selected and the /CS pin is high, the following pins become high impedance.</p> <ol style="list-style-type: none"> In 8-bit parallel: D15-D8 pins are in the state of high impedance should connect to VDD. In 3-line/4-line interface D0 pad will be used for SI function In 4-line interface D1 pad will be used for A0 function In Serial interface: unused pins are in the state of high impedance should connect to VDD. 		
SI	I	<p>SI is used to input serial data when the serial interface is selected.(3 line and 4 line)</p> <p>It is used by "D0" pad, See Table 7.2-1.</p>		
SCL	I	<p>SCL is used to input serial clock when the serial interface is selected.</p> <p>The data is converted in the rising edge. (3 line and 4 line)</p> <p>It is used by "A0" pad , See Table 7.2-1.</p>		
TE	O	Tearing effect output.		

ST7637

/EXT	I	<p>OTP burn-in control Pin.</p> <p>There is a pull-high resistor between /EXT & VDD in ST7637.</p> <p>When burning OTP, please add an external VSS on /EXT. (needs external power supply voltage VPP=7.5V~7.75V)</p>
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NOTE:

1. Microprocessor interface pins should not be floating in any operation mode.
2. Unused pin should connect to VDD (Supply Digital Voltage).

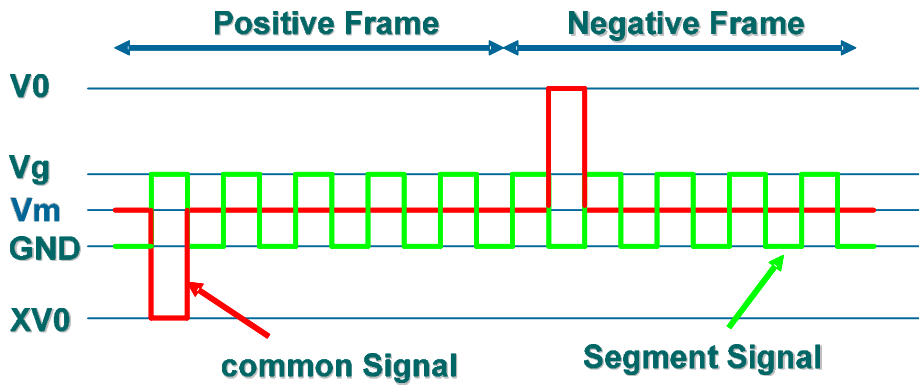
6.5 LCD DRIVER OUTPUTS

Name	I/O	Description																										
SEG0 to SEG395	O	<p>LCD segment driver outputs</p> <p>The display data and the M signal control the output voltage of segment driver.</p> <table border="1"> <thead> <tr> <th rowspan="2">Display data</th> <th rowspan="2">M (Internal)</th> <th colspan="2">Segment driver output voltage</th> </tr> <tr> <th>Normal display</th> <th>Reverse display</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>Vg</td> <td>VSS</td> </tr> <tr> <td>H</td> <td>L</td> <td>VSS</td> <td>Vg</td> </tr> <tr> <td>L</td> <td>H</td> <td>VSS</td> <td>Vg</td> </tr> <tr> <td>L</td> <td>L</td> <td>Vg</td> <td>VSS</td> </tr> <tr> <td colspan="2">Sleep-In mode</td> <td>VSS</td> <td>VSS</td> </tr> </tbody> </table>	Display data	M (Internal)	Segment driver output voltage		Normal display	Reverse display	H	H	Vg	VSS	H	L	VSS	Vg	L	H	VSS	Vg	L	L	Vg	VSS	Sleep-In mode		VSS	VSS
Display data	M (Internal)	Segment driver output voltage																										
		Normal display	Reverse display																									
H	H	Vg	VSS																									
H	L	VSS	Vg																									
L	H	VSS	Vg																									
L	L	Vg	VSS																									
Sleep-In mode		VSS	VSS																									
COM0 to COM131	O	<p>LCD common driver outputs</p> <p>The internal scanning data and M signal control the output voltage of common driver.</p> <table border="1"> <thead> <tr> <th>Scan data</th> <th>M (Internal)</th> <th>Common driver output voltage</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>XV0</td> </tr> <tr> <td>H</td> <td>L</td> <td>V0</td> </tr> <tr> <td>L</td> <td>H</td> <td>Vm</td> </tr> <tr> <td>L</td> <td>L</td> <td>Vm</td> </tr> <tr> <td colspan="2">Sleep-In mode</td> <td>VSS</td> </tr> </tbody> </table>	Scan data	M (Internal)	Common driver output voltage	H	H	XV0	H	L	V0	L	H	Vm	L	L	Vm	Sleep-In mode		VSS								
Scan data	M (Internal)	Common driver output voltage																										
H	H	XV0																										
H	L	V0																										
L	H	Vm																										
L	L	Vm																										
Sleep-In mode		VSS																										

Name	I/O	Description
DETGBI DETGBO	ITO	DETGBI must connect to DETGBO by ITO which run a ring on LCM glass.

ST7637

Driving Waveform



ST7637 I/O PIN ITO Resister Limitation

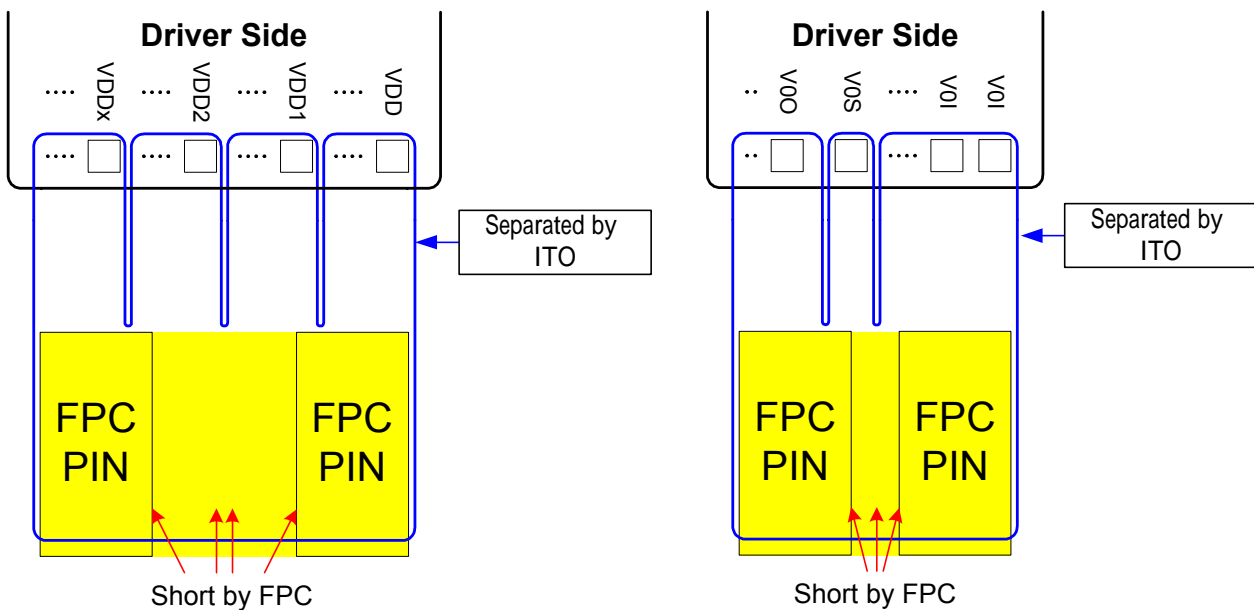
Pin Name	ITO Resister
VDD, VDD1~VDD5, VSS,VSS1,VSS2,VSS4,SI(in serial interface is D0)	<100Ω
V0 _{IN} , V0 _{OUT} , V0 _S , XV0 _{IN} , XV0 _{OUT} , XV0 _S , Vg _{IN} , Vg _{OUT} , Vg _S , Vm	<300Ω
VPP	<50Ω
A0, E_RD, RW_WR, /CS, D0(in pallel interface),D1, ...D15, (SCL), TE	<1KΩ
/RST	<10KΩ
IF[3:1], CLS, CSEL, /EXT	<1KΩ
TCAP, CL, VREF	Floating

NOTE:

1. Make sure that the ITO resistance of COM0 ~ COM131 is equal, and so is it of SEG0 ~ SEG395.

These limitations include the bottleneck of ITO layout.

2. ITO layout suggestion is shown as below:



7. FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

/CS pin is chip selection. The ST7637 is active when /CS=L. In serial interface mode, the internal shift register and the counter are reset when /CS=H.

7.2 Selecting Parallel / Serial Interface

ST7637 has six types of interfaces with an MPU, which are two serial and four parallel interfaces. These parallel or serial interfaces are determined by IF pin as shown in Table 7.2-1.

I/F Mode			I/F Description	Pin Assignment						
IF3	IF2	IF1		/CS	A0	E_RD	RW_WR	Used Data Bus	D1	D0
H	H	H	80 serial 16-bit parallel	/CS	A0	/RD	/WR	D15~D2	D1	D0
H	H	L	80 serial 8-bit parallel	/CS	A0	/RD	/WR	D7~D2	D1	D0
H	L	H	68 serial 16-bit parallel	/CS	A0	E	R/W	D15~D2	D1	D0
H	L	L	68 serial 8-bit parallel	/CS	A0	E	R/W	D7~D2	D1	D0
L	H	H	8-bit SPI mode (4 line)	/CS	SCL	--	--	--	A0	SI
L	H	L	9-bit SPI mode (3 line)	/CS	SCL	--	--	--	--	SI

Table 7.2-1 Parallel / Serial Interface Mode

NOTE: When these pins are set to any other combination, A0, E_RD and RW_WR inputs are disabled and D0 to D15 are to be high impedance.

7.2.1. 8-bit or 16-bit Parallel Interface

The ST7637 identifies the type of the data bus signals according to the combination of A0, /RD (E) and /WR (W/R) signals, as shown in Table 7.2-2.

Common	6800-series		8080-series		Description	
	A0	RW	E	/WR		/RD
H	H	H	↑	H	↓	Display data read out
H	H	L	↑	H	↓	Register status read
L	L	H	↓	↑	H	Instruction write
H	L	L	↓	↑	H	Display data write

Table 7.2-2 Parallel Data Transfer

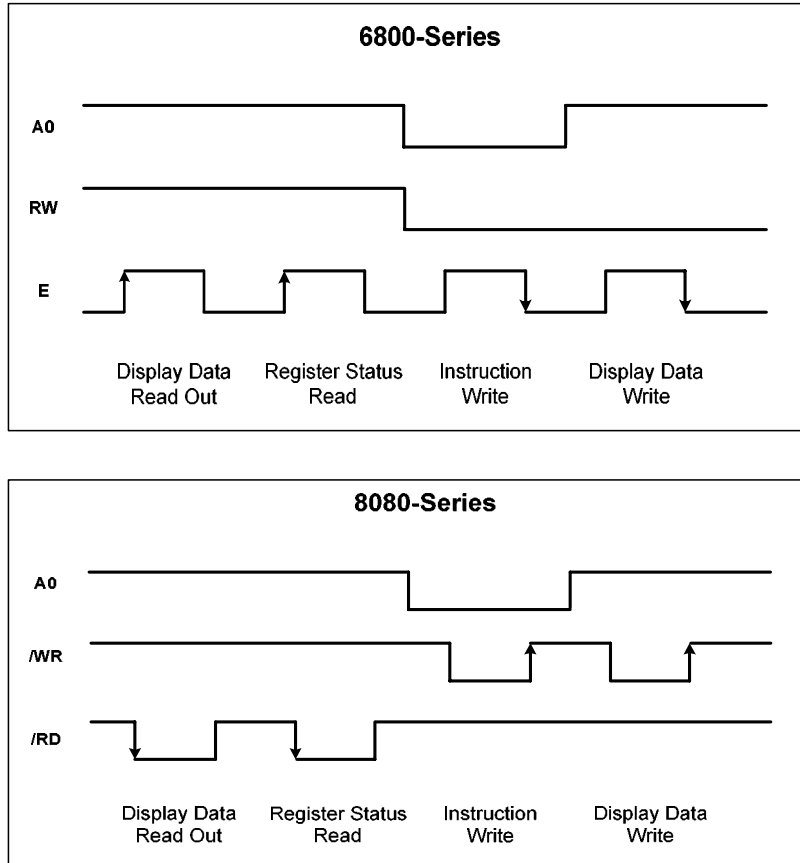


Figure 7.2-3 Parallel Data Transfer Example Chart

Relation between Data Bus and Gradation Data

ST7637 offers 256 color, 4096 color display, 65K color display, and truncated 262K color display, truncated 16M color display. When using 256 colors, 4096, 65K, 262K, and 16M color display; you can specify color for each of R, G, and B using the palette function. Use the command for switching between these modes.

(1) 256 color input mode

1. 8-bit interface

D7, D6, D5, D4, D3, D2, D1, D0: RRRGGGBB 1st -write

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st -write operation finishes.

2. 16-bit interface

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: XXXXXXXXRRRGGGBB 1st -write

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st -write operation finishes. "X" are ignored dummy bits.

(2) 4096-color display

(1-1) Type A 4096 color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: **RRRRGGGG** 1st-write

D7, D6, D5, D4, D3, D2, D1, D0: **BBBBRRRR** 2nd-write

D7, D6, D5, D4, D3, D2, D1, D0: **GGGGBBBB** 3rd-write

There are 3 write operations for 2 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes, and 2nd pixel data is written in the display data RAM when 3rd–write operation finishes.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: **RRRRGGGGBBBBXXXX** 1st-write

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes. “X” are ignored dummy bits.

(1-2) Type B 4096 color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: **XXXXRRRR** 1st-write

D7, D6, D5, D4, D3, D2, D1, D0: **GGGGBBBB** 2nd-write

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes. “X” are ignored dummy bits.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: **XXXXRRRRGGGGBBBB** 1st-write

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes. “X” are ignored dummy bits.

(3) 65K color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: **RRRRGGGG** 1st-write

D7, D6, D5, D4, D3, D2, D1, D0: **GGBBBBBB** 2nd-write

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: **RRRRGGGGGGBBBBBB**

There is only 1 write operation for 1 pixel data.

1 pixel data is written in the display data RAM when 1st –write operation finishes.

(4) Truncated 262K color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: **RRRRRRXX** 1st-write

D7, D6, D5, D4, D3, D2, D1, D0: **GGGGGGXX** 2nd-write

D7, D6, D5, D4, D3, D2, D1, D0: **BBBBBBXX** 3rd-write

There are 3 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 3rd–write operation finishes. “X” are ignored dummy bits.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: **RRRRRRXXGGGGGGXX** 1st-write

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: **BBBBBBXXXXXXXXXX** 2nd-write

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes. “X” are ignored dummy bits.

(5) Truncated 16M color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: **RRRRRRRR** 1st-write

D7, D6, D5, D4, D3, D2, D1, D0: **GGGGGGGG** 2nd-write

D7, D6, D5, D4, D3, D2, D1, D0: **BBBBBBBB** 3rd-write

There are 3 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 3rd–write operation finishes. “X” are ignored dummy bits.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: **RRRRRRRRGGGGGGGG** 1st-write

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: **BBBBBBBBXXXXXXXX** 2nd-write

There are 2 write operations for 1 pixel data.

1st pixel data is written in the display data RAM when 2nd –write operation finishes. “X” are ignored dummy bits.

NOTE: 7637 offer read DDRAM function only in 65K color mode.

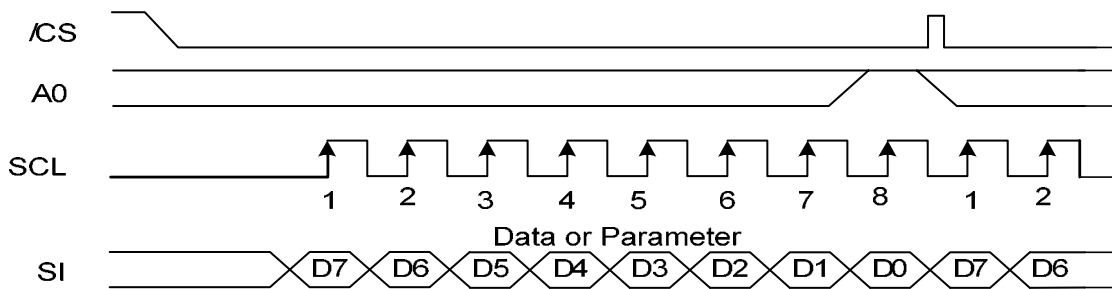
7.2.2. 8- and 9-bit Serial Interface

The 8-bit serial interface uses four pins /CS, SI, SCL, and A0 to write in commands and data. Meanwhile, the 9-bit serial interface uses three pins /CS, SI and SCL for the same purpose.

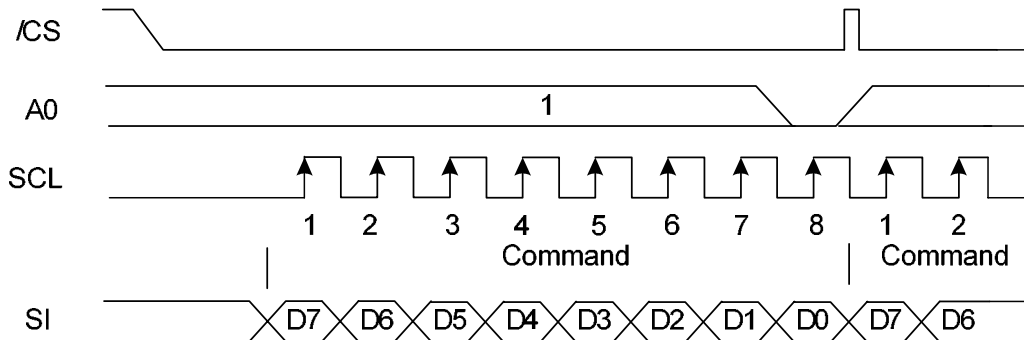
Data read is not available in the serial interface. Data must write to IC with 8 bits for each time. The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4-line)

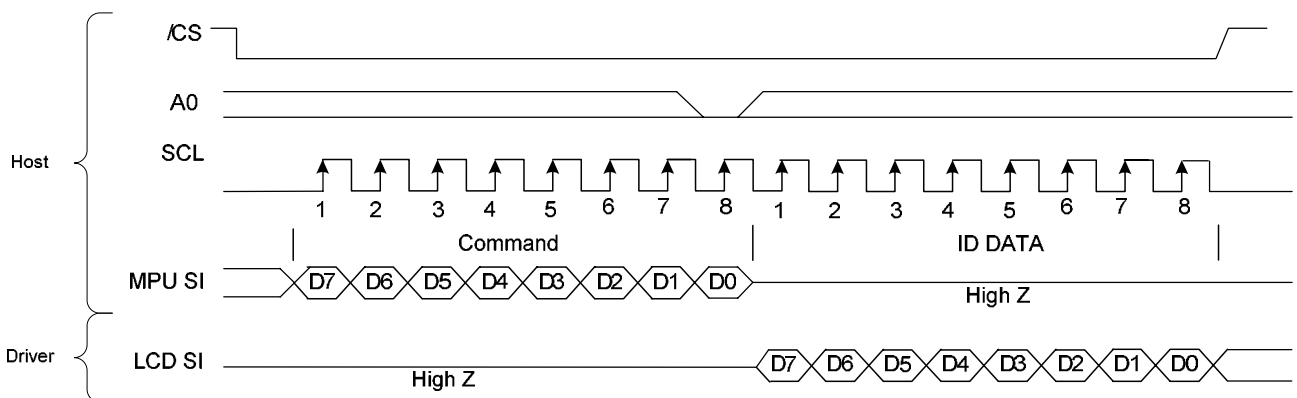
When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.



When entering command: A0= LOW at the rising edge of the 8th SCL

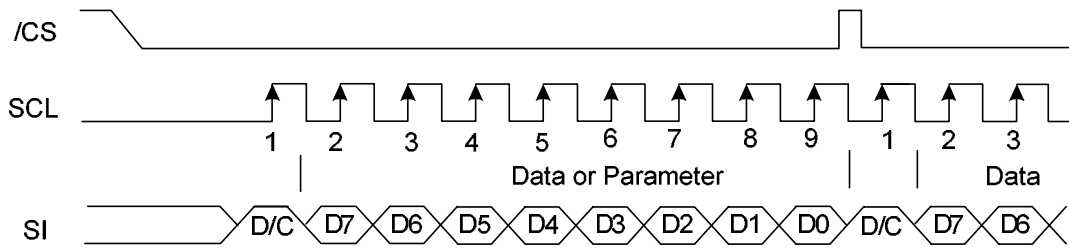


When entering reading command:

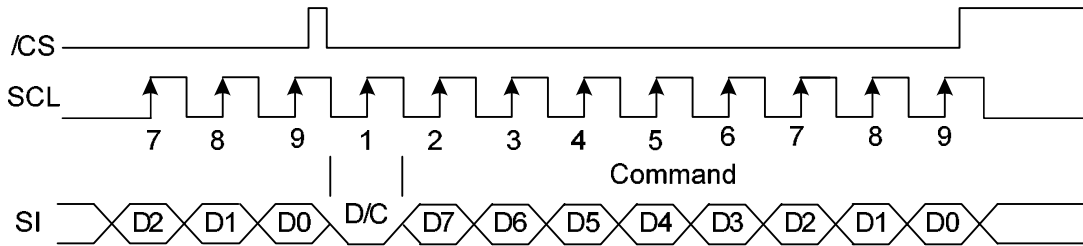


(2) 9-bit serial interface (3-line)

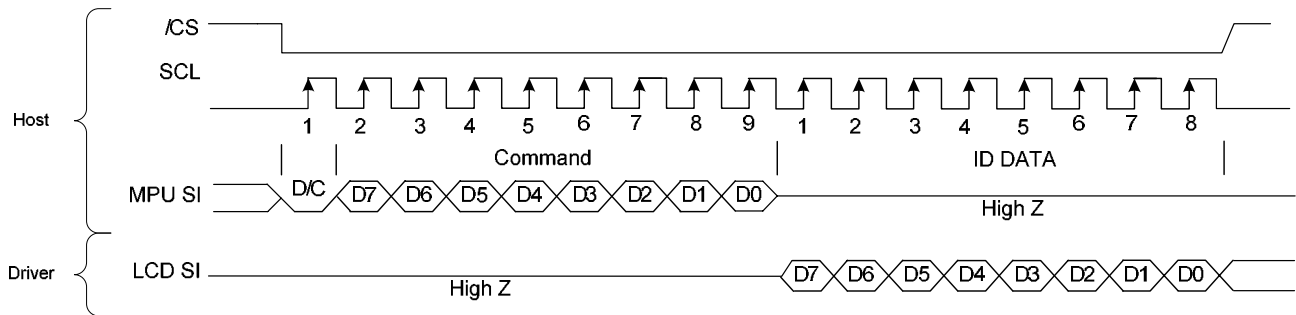
When entering data (parameters): SI= HIGH at the rising edge of the 1st SCL.



When entering command: SI= LOW at the rising edge of the 1st SCL.



When entering reading command:



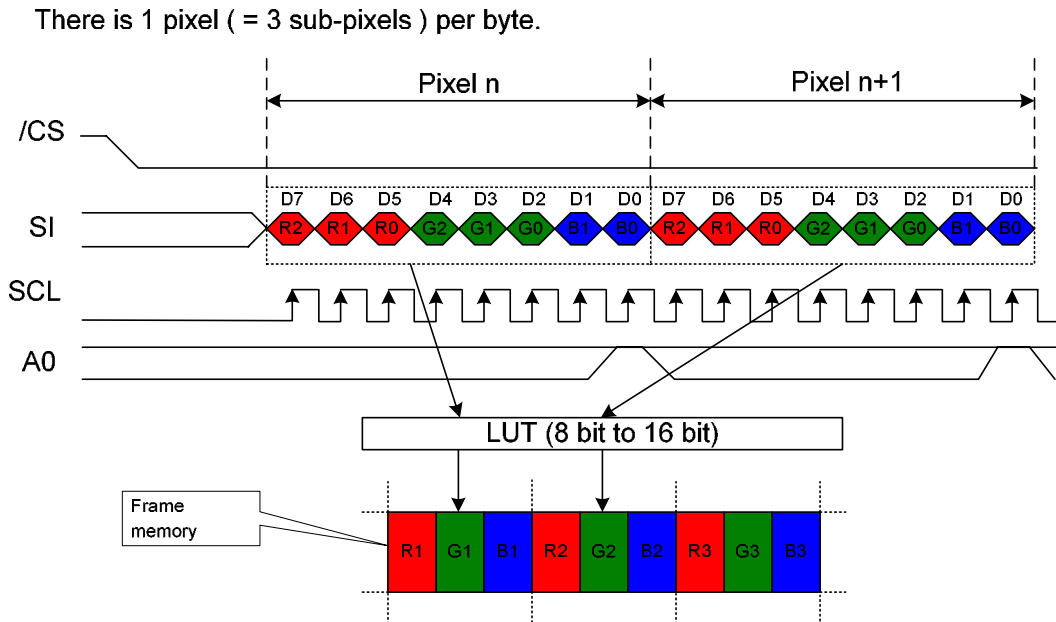
- If /CS is set to HIGH while the 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set /CS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.

7.2.3. 8-bit and 9-bit Serial Interface Data Color Coding

8-bit serial interface (4-line)

(1) R 3-bit, G 3-bit, B 2-bit, 256 colors

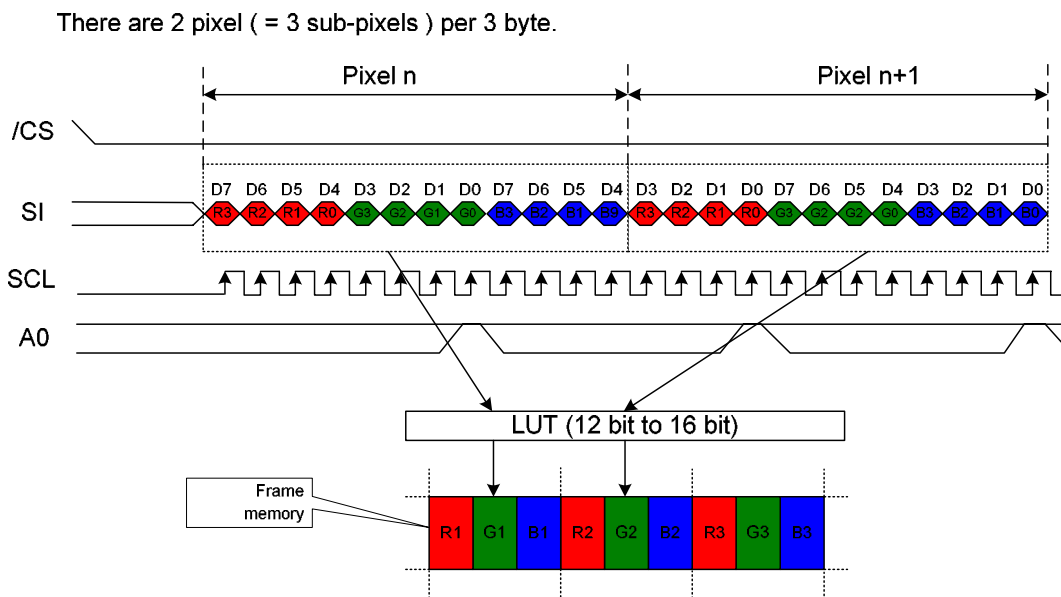
There is 1 pixel (= 3 sub-pixels) per byte.



Note: R2, G2, B1 are the most significant bits and R0, G0, B0 are the least significant bits.

(2) R 4-bit, G 4-bit, B 4-bit, 4,096 colors — Type A

There are 2 pixel (= 3 sub-pixels) per 3 byte.



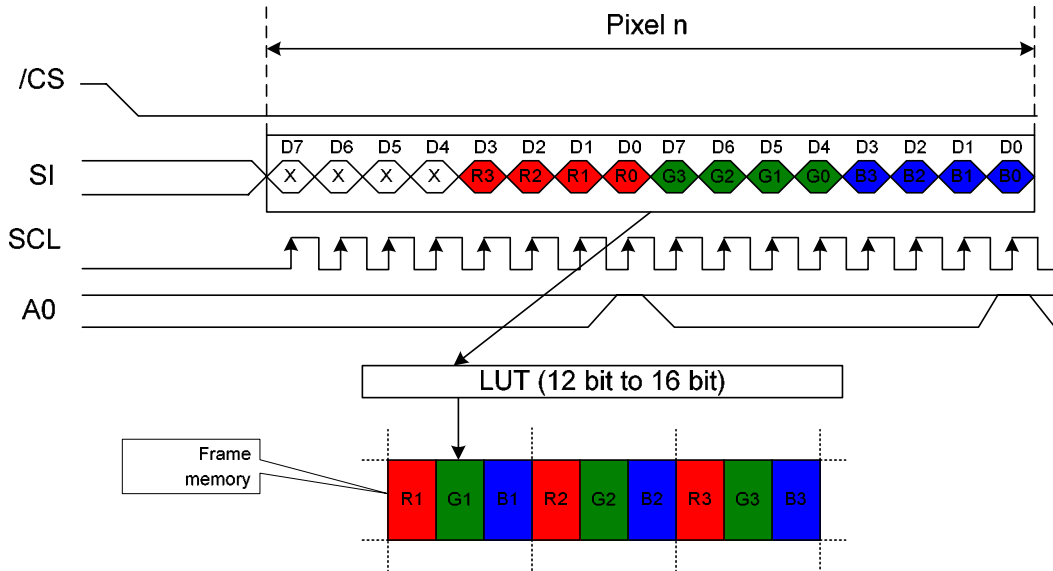
Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

ST7637

(3) R 4-bit, G 4-bit, B 4-bit, 4,096 colors — Type B

There is 1 pixel (= 3 sub-pixels) per 2 bytes.

There is 1 pixel (= 3 sub-pixels) per 2 bytes.

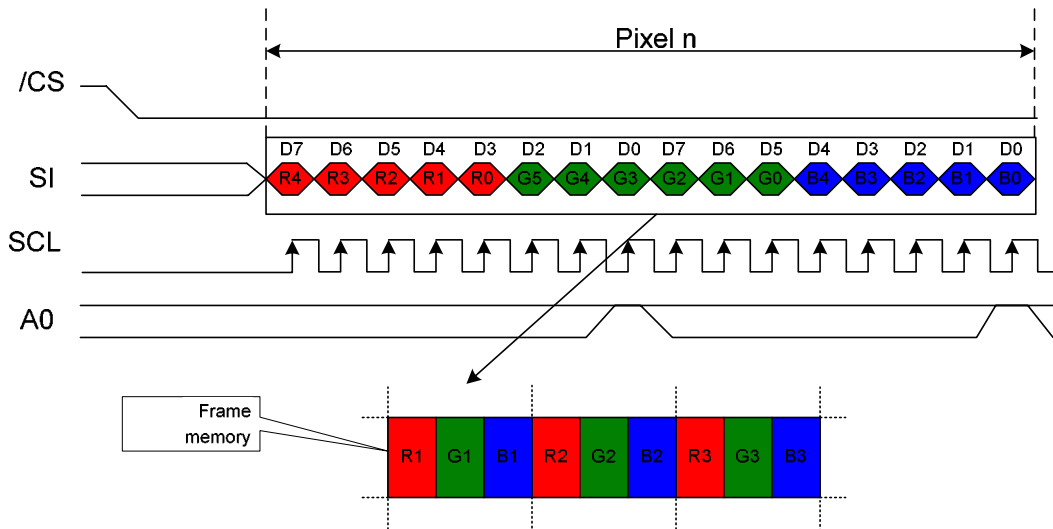


Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(4) R 5-bit, G 6-bit, B 5-bit, 65,536 colors

There is 1 pixel (= 3 sub-pixels) per 2 byte.

There is 1 pixel (= 3 sub-pixels) per 2 byte.



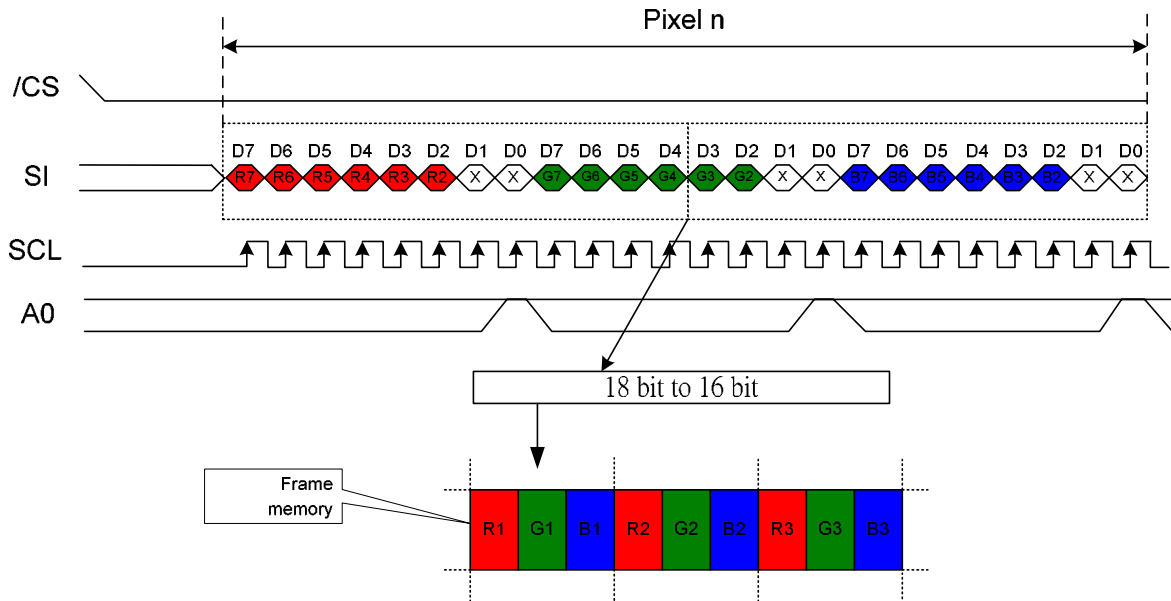
Note: R4, G5, B4 are the most significant bits and R0, G0, B0 are the least significant bits.

ST7637

(5) R 5-bit, G 6-bit, B 5-bit, 262,144 colors

There is 1 pixel (= 3 sub-pixels) per 3 byte.

There is 1 pixel (= 3 sub-pixels) per 3 byte.

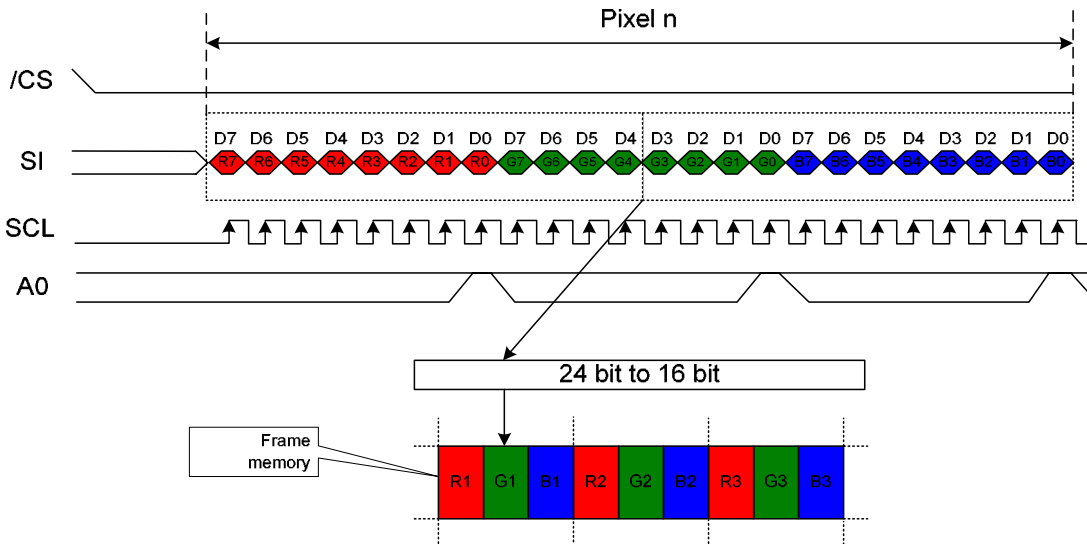


Note: R7, G7, B7 are the most significant bits and R2, G2, B2 are the least significant bits.

(6) R 8-bit, G 8-bit, B 8-bit, 16M colors

There is 1 pixel (= 3 sub-pixels) per 3 byte.

There is 1 pixel (= 3 sub-pixels) per 3 byte.

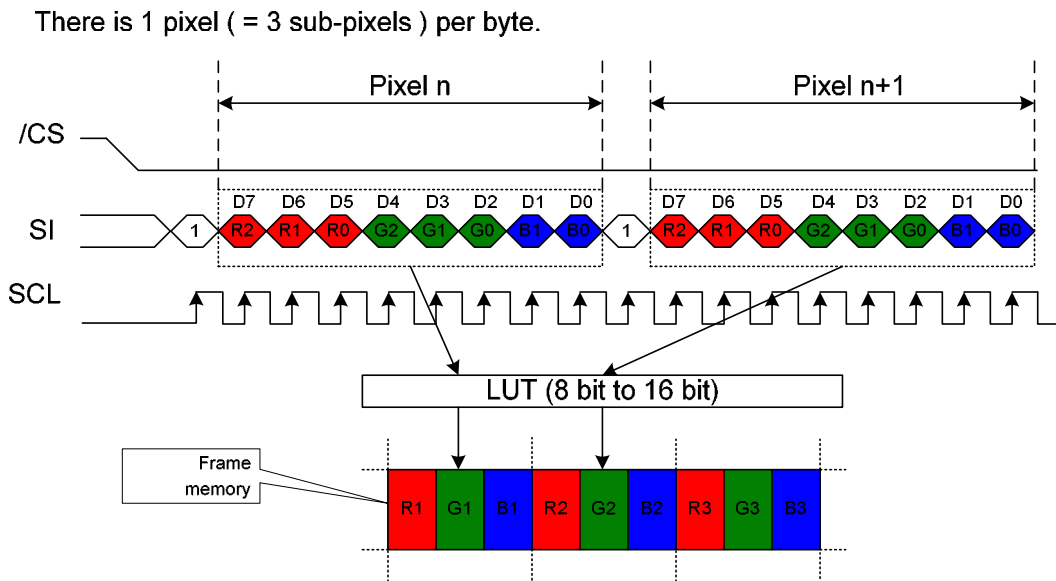


Note: R7, G7, B7 are the most significant bits and R0, G0, B0 are the least significant bits.

9-bit serial interface (3-line)

(1) R 3-bit, G 3-bit, B 2-bit, 256 colors

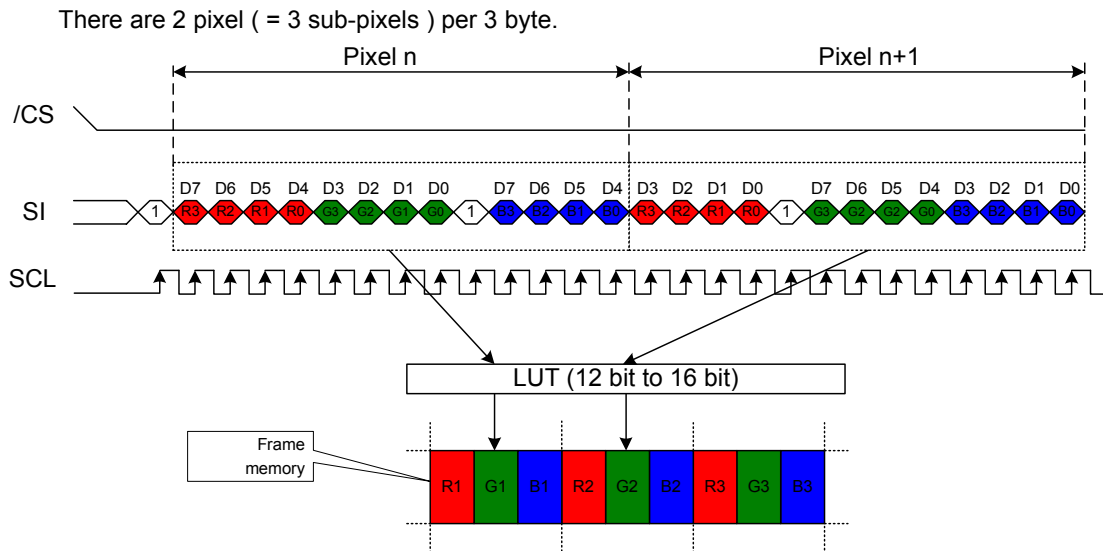
There is 1 pixel (= 3 sub-pixels) per byte.



Note: R2, G2, B1 are the most significant bits and R0, G0, B0 are the least significant bits.

(2) R 4-bit, G 4-bit, B 4-bit, 4,096 colors – Type A

There are 2 pixel (= 3 sub-pixels) per 3 byte.



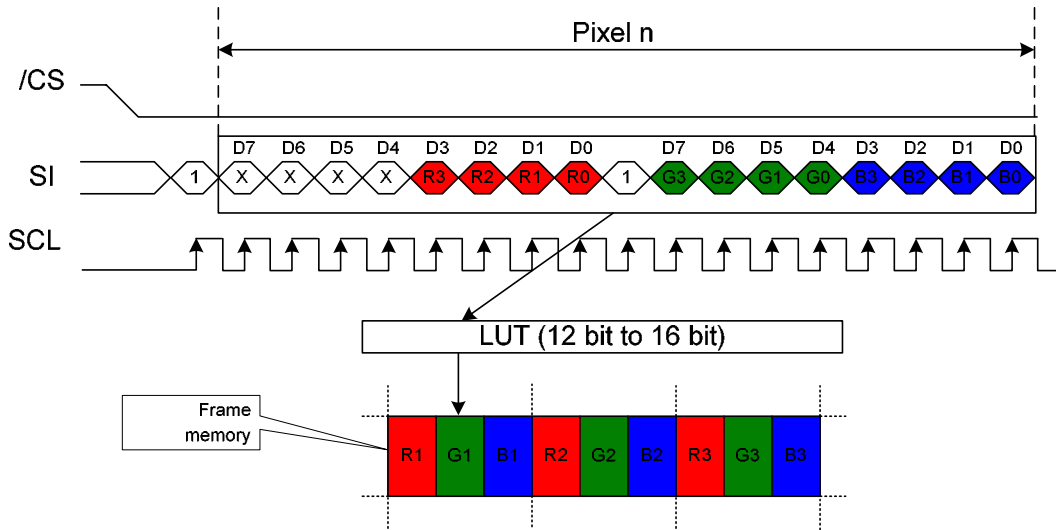
Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

ST7637

(3) R 4-bit, G 4-bit, B 4-bit, 4,096 colors – Type B

There is 1 pixel (= 3 sub-pixels) per 2 bytes.

There is 1 pixel (= 3 sub-pixels) per 2 bytes.

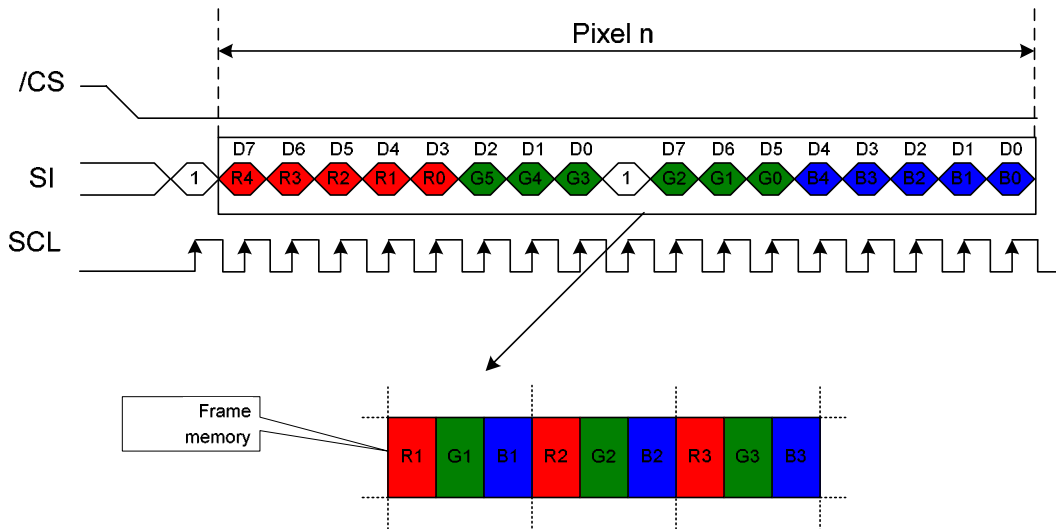


Note: R3, G3, B3 are the most significant bits and R0, G0, B0 are the least significant bits.

(4) R 5-bit, G 6-bit, B 5-bit, 65,536 colors

There is 1 pixel (= 3 sub-pixels) per 2 byte.

There is 1 pixel (= 3 sub-pixels) per 2 byte.



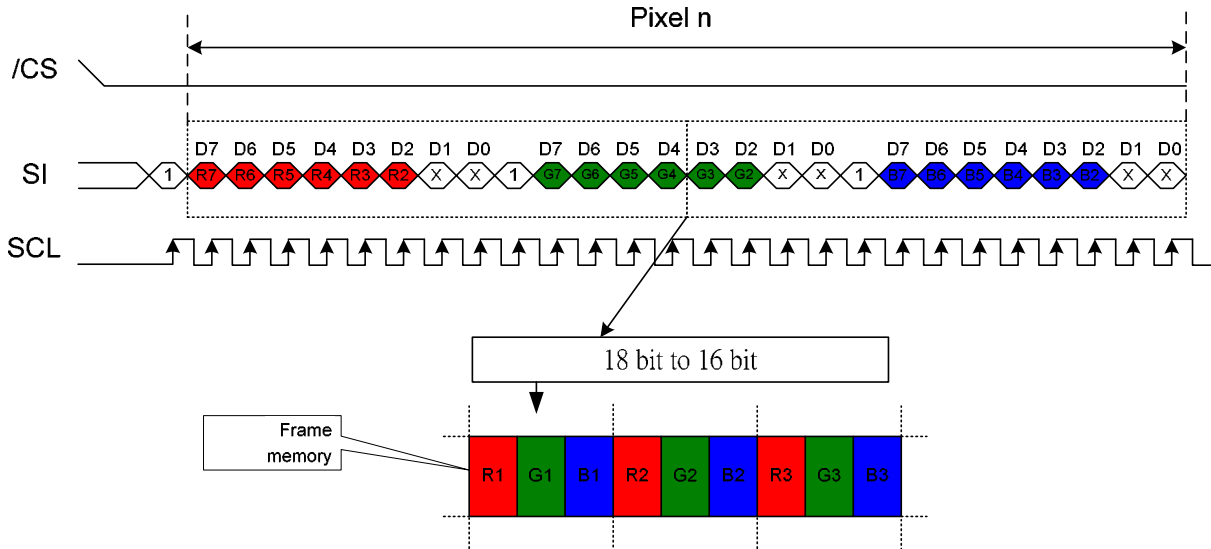
Note: R4, G5, B4 are the most significant bits and R0, G0, B0 are the least significant bits.

ST7637

(5) R 5-bit, G 6-bit, B 5-bit, 262,144 colors

There is 1 pixel (= 3 sub-pixels) per 3 byte.

There is 1 pixel (= 3 sub-pixels) per 3 byte.

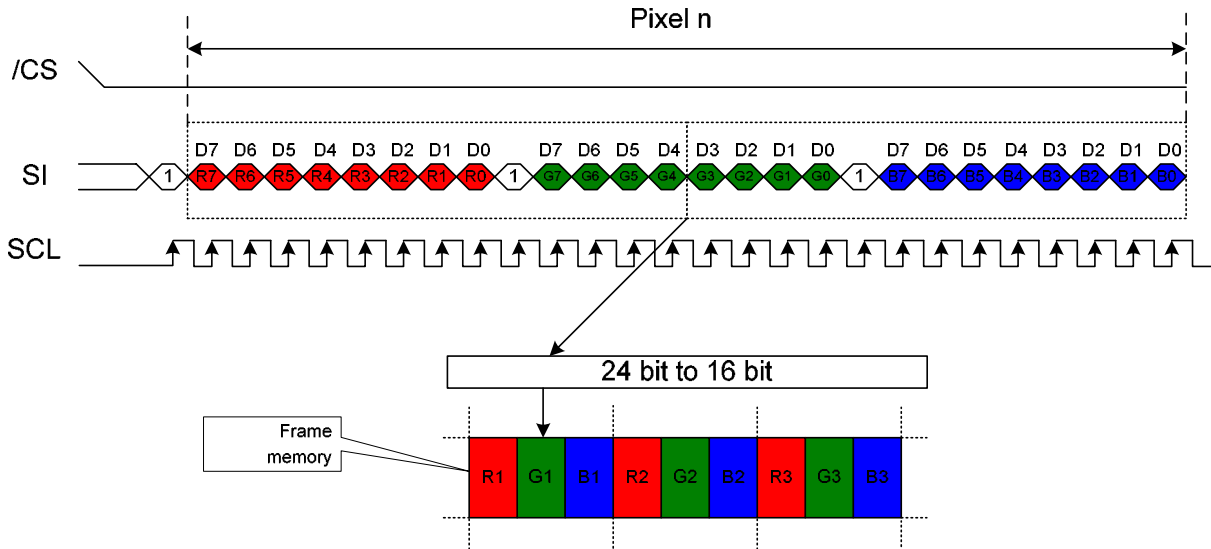


Note: R7, G7, B7 are the most significant bits and R2, G2, B2 are the least significant bits.

(6) R 8-bit, G 8-bit, B 8-bit, 16M colors

There is 1 pixel (= 3 sub-pixels) per 3 byte.

There is 1 pixel (= 3 sub-pixels) per 3 byte.



Note: R7, G7, B7 are the most significant bits and R0, G0, B0 are the least significant bits.

7.3 ACCESS TO DDRAM AND INTERNAL REGISTERS

ST7637 realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle. Figure 7.3-1 illustrates these relations.

In 80-series interface mode:

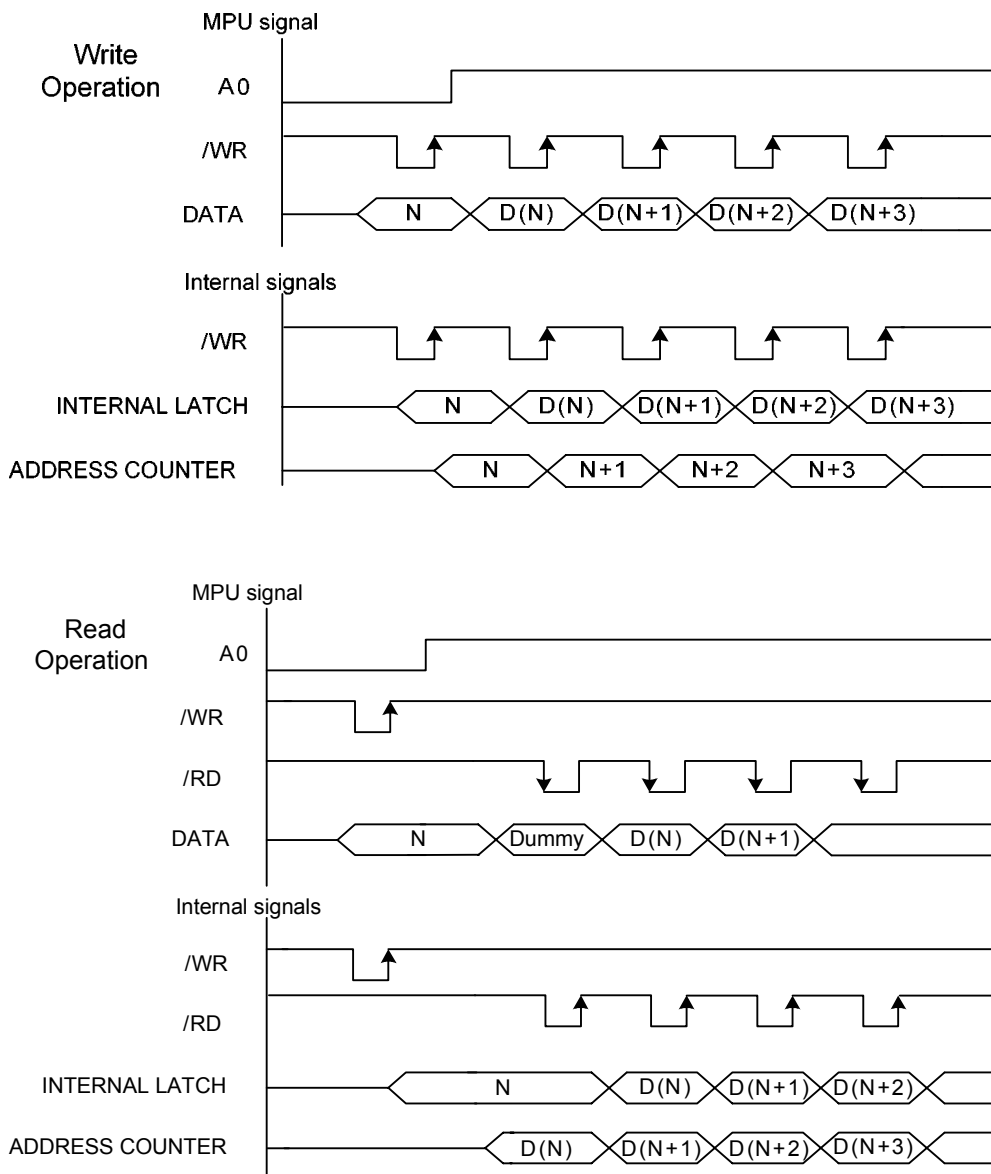


Figure 7.3-1

ST7637

7.4 DISPLAY DATA RAM (DDRAM)

7.4.1. DDRAM

It is 132 X 132 X 16 bits capacity RAM prepared for storing dot data. Refer to the following memory map for the RAM configuration.

Memory Map

		RGB alignment									
Data control command		Column									
	(MADCTR) MX=0	0	1							131	
	(MADCTR) MX=1	131	130							0	
	Color	R	G	B	R	G	B		R	G	B
	Data										
	Page										
	(MADCTR) MY=0										
	(MADCTR) MY=1										
0	131										
1	130										
2	129										
3	128										
4	127										
5	126										
6	125										
7	124										
:	:										
124	7										
125	6										
126	5										
127	4										
128	3										
129	2										
130	1										
131	0										
SEGout		0	1	2	3	4	5		393	394	395

You can change position of R and B with MADCTR command.

7.4.2. Address Control

The address counter sets the addresses of the display data RAM for writing.

Data is written pixel into the RAM matrix of ST7637. The data for one pixel or two pixels is collected (RGB 5-6-5-bit), according to the data formats. As soon as this pixel-data information is complete, the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=131 (83h) and Y=0 to Y=131 (83h). Addresses outside these ranges are not allowed.

Before writing to the RAM, a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=131 (83h), YE=131 (83h).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (MV=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS). For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTR", define flags MV, MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Figure 7.4-1 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 7.4-1 Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

7.4.3. I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM when the LCD is turned on does not cause troubles such as flicking of the display images.

7.4.4. Scroll Address Circuit

The circuit associates lines on DDRAM with COM output. ST7637 processes signals for the liquid crystal display on 1-line basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in line.

7.4.5. Display data Latch Circuit

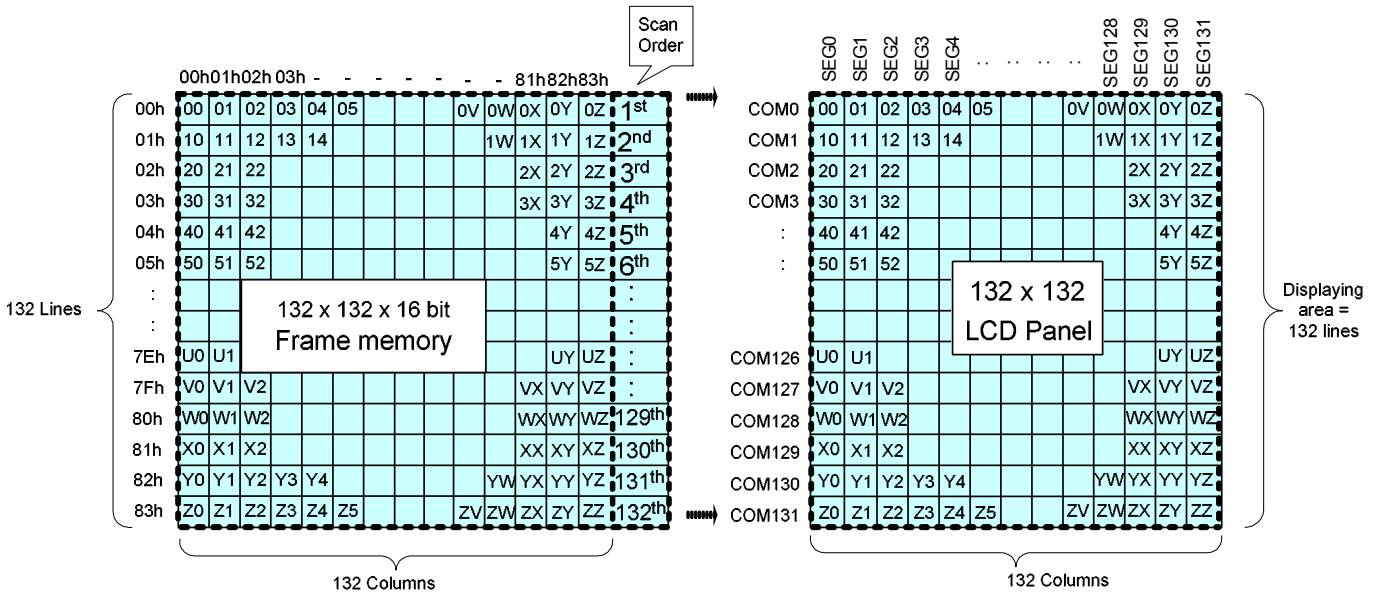
This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

7.4.6. Normal Display On or Partial Mode On, Vertical Scroll Off

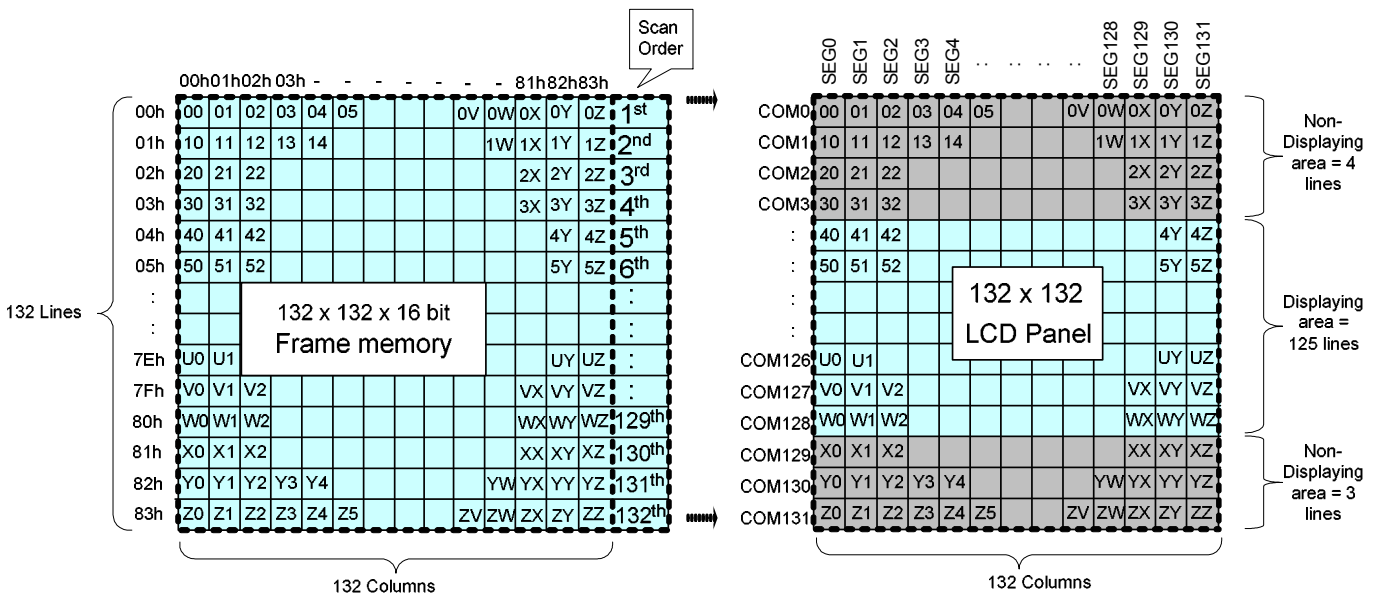
In this mode, contents of the frame memory within an area where column address is 00h to 83h and row address is 00h to 83h is displayed.

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).

Example1) Normal Display On



Example2) Partial Display On: PSL[6:0] = 04h, PEL[6:0] = 80h, MADCTR (ML)=0



7.4.7. Vertical Scroll/Rolling Scroll

7.4.7.1. Rolling Scroll

There is just one types of vertical scrolling, which are determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

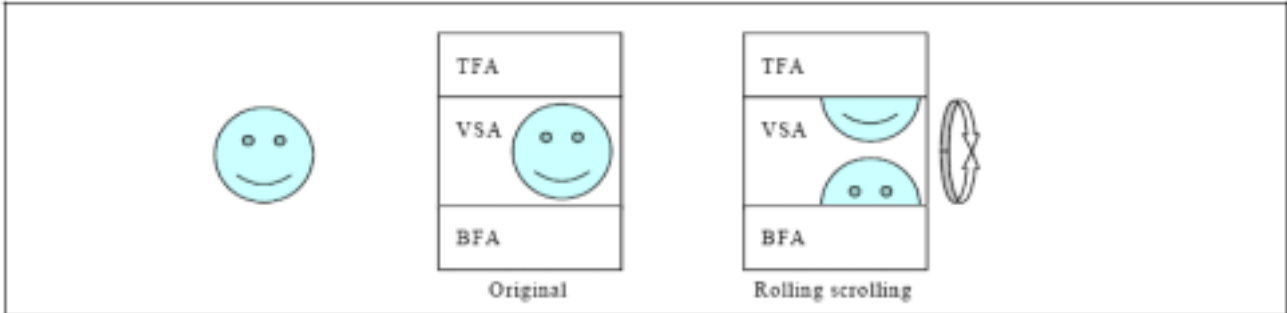
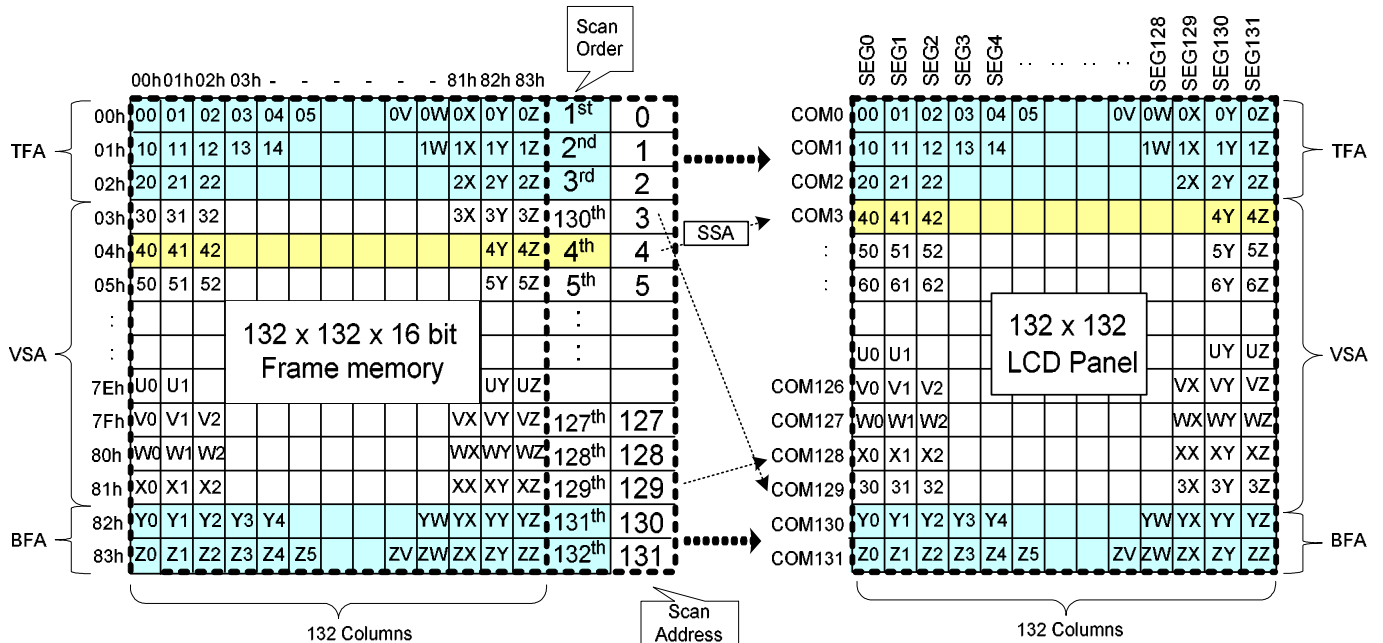


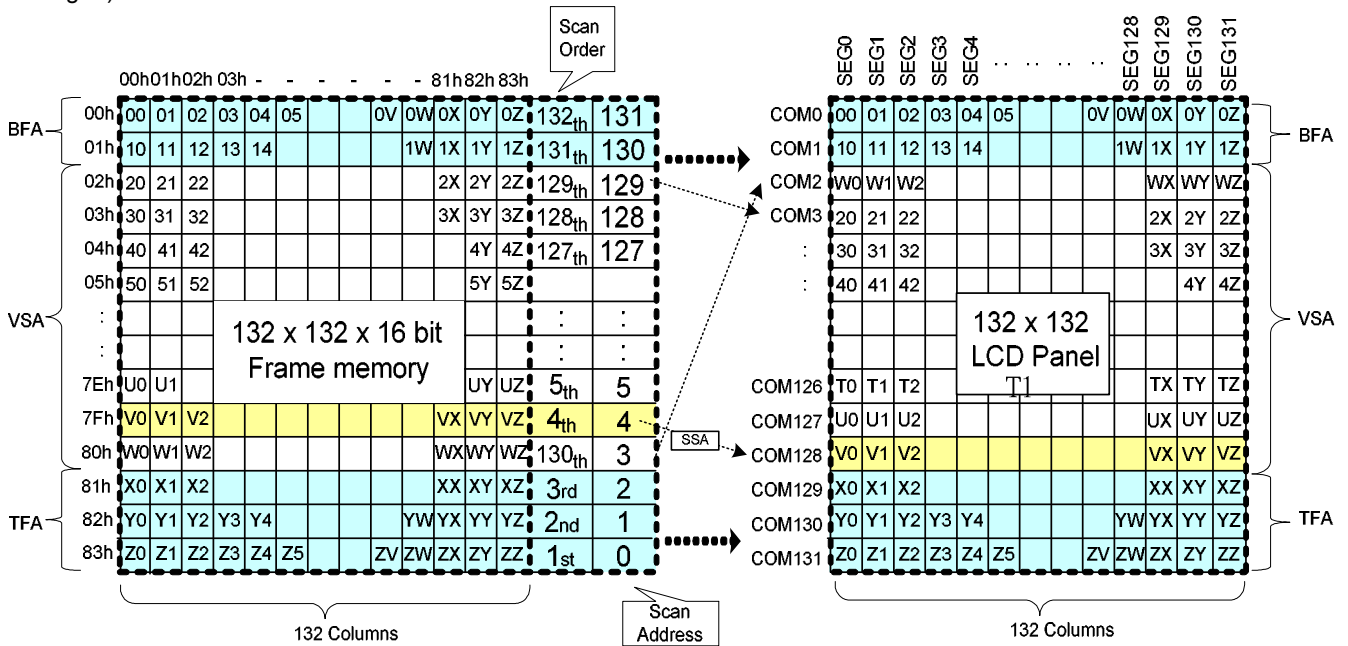
Figure 7.4-2 Rolling Scroll Definition

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =132. In this case, 'rolling' scrolling is applied as shown below. All the memory contents will be used.

Example1) Panel size=132 x 132, TFA =3, VSA=127, BFA=2, SSA=4, MADCTR ML=0: Rolling Scroll



Example2) Panel size=132 x 132, TFA =3, VSA=127, BFA=2, SSA=4, MADCTR ML=1: Rolling Scroll (TFA and BFA are exchanged)



7.4.7.2. Vertical Scroll Example

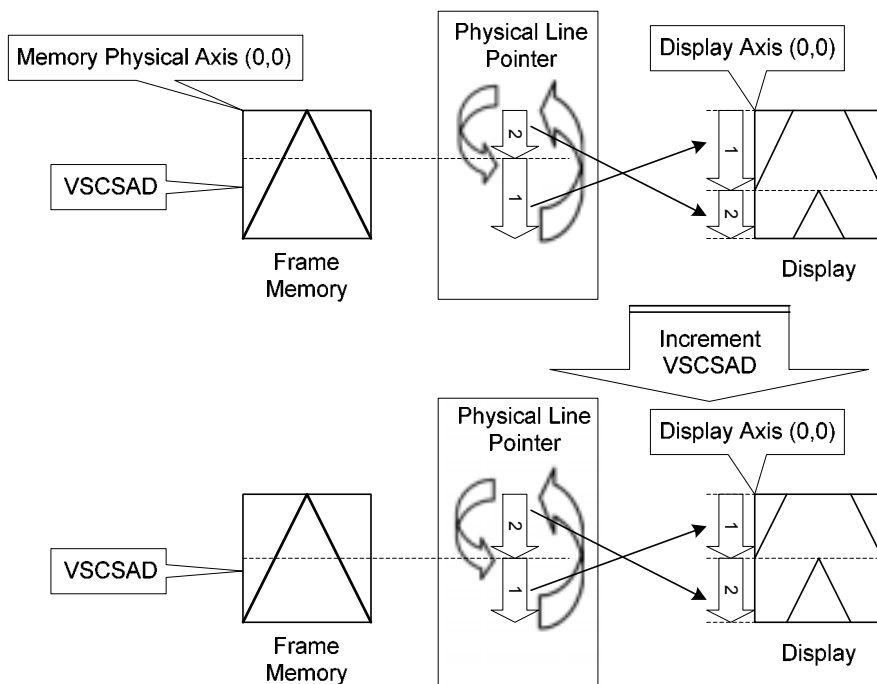
There are 2 types of vertical scrolling, which are determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: $TFA + VSA + BFA < 132$

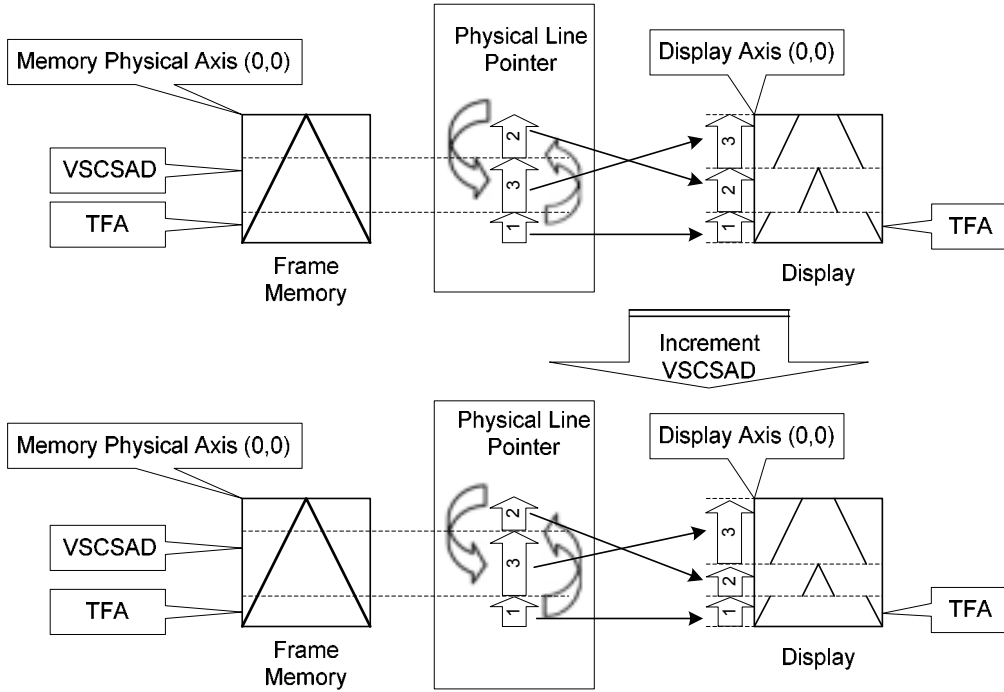
N/A. Do not set $TFA + VSA + BFA < 132$. In that case, unexpected picture will be shown.

Case 2: $TFA + VSA + BFA = 132$ (Rolling Scrolling)

Example1) When MADCTR parameter ML="0", TFA=0, VSA=132, BFA=0 and VSCSAD=40.



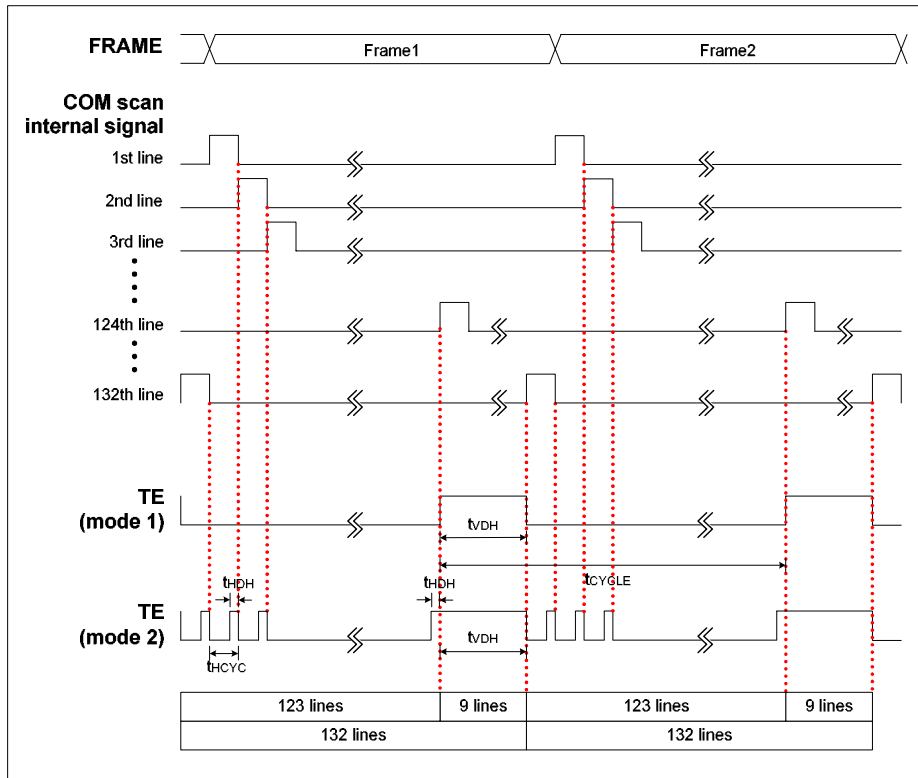
Example2) When MADCTR parameter ML="1", TFA=10, VSA=122, BFA=0 and VSCSAD=30.



7.4.8. Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

7.4.8.1. Tearing Effect Line Modes



Mode 1, the Tearing Effect Output signal consists of V-Sync (t_{VDH}) information. It starts at 124th line signal and ends at the 132th line signal. There is one high pulse during each frame.

Mode 2, the Tearing Effect Output signal consists of both H-Sync(t_{HDH}) and V-Sync(t_{VDH}) information. TE pin outputs t_{HDH} pulse on each COM scan signal. During 124th ~ 132th line signal, it output a high pulse which equals:

$1 t_{HDH} + 1 t_{VDH}$.

Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

7.4.8.2. Tearing Effect Line Timing

The Tearing Effect signal is described below:

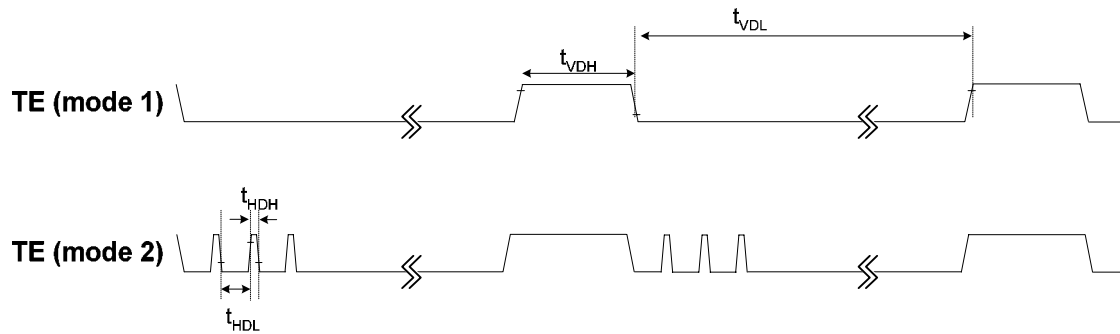
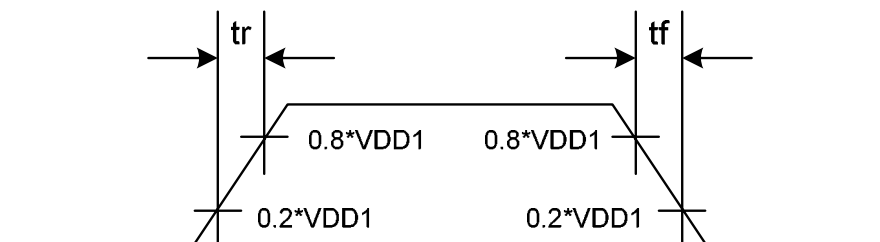


Figure 7.4-3 AC characteristics of Tearing Effect Signal

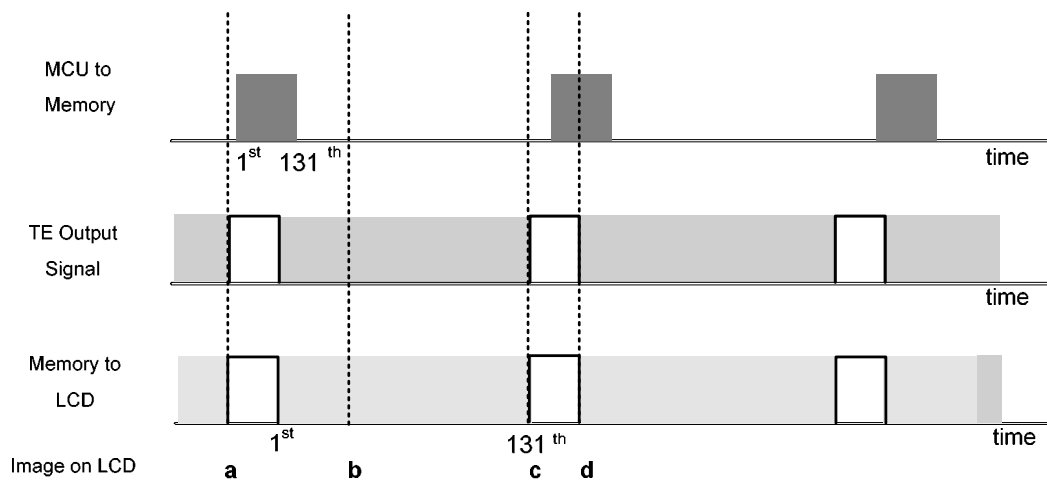
Idle Mode Off (Frame Rate = 77Hz)

Symbol	Parameter	Min	Typ	Max	Unit	Description
t _{VDL}	Vertical Timing Low Duration	--	11.4	--	ms	Mode1
t _{VDH}	Vertical Timing High Duration	1	1.6	--	ms	
t _{HDL}	Horizontal Timing Low Duration	-	92	--	us	Mode2
t _{HDH}	Horizontal Timing High Duration	3	6	--	us	

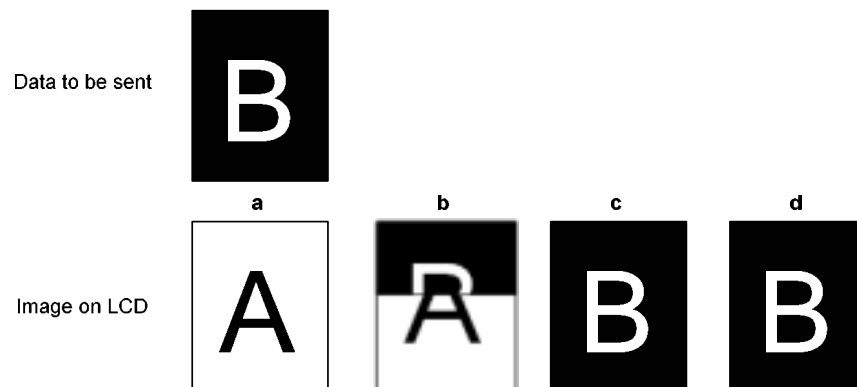
Note: The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



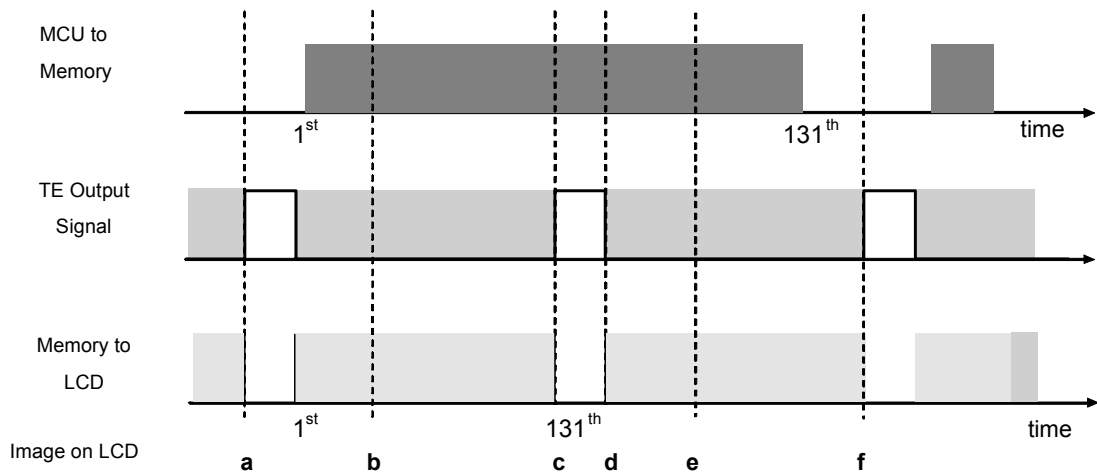
Example 1: MPU Write is faster than Panel Read.



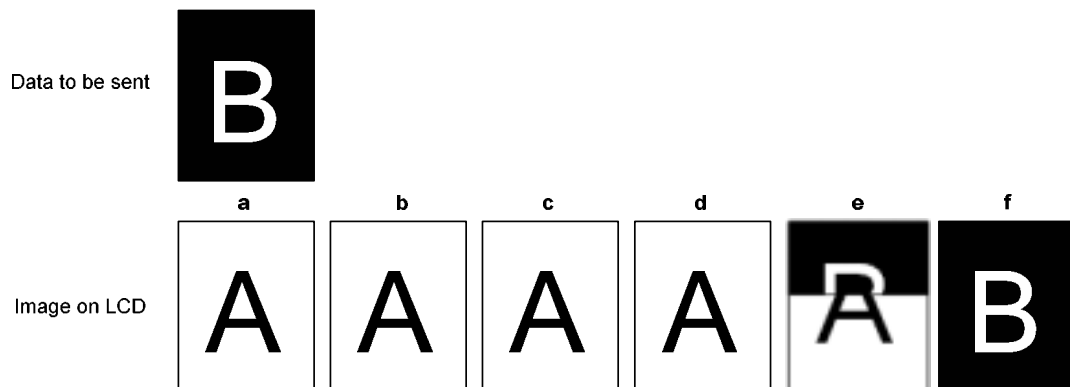
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



Example 2: MPU Write is slower than Panel Read.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



7.5 Gray-Scale Display

ST7637 incorporates a 4FRC & 31 PWM function circuit to display a 64 gray-scale display.

7.6 Oscillation circuit

This is on-chip oscillator without external resistor. When the internal oscillator is used, CLS must connect to VDD; when the external oscillator is used, CL could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

7.7 Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock CL (internal), which is generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 132-bits display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M), which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.7-1.

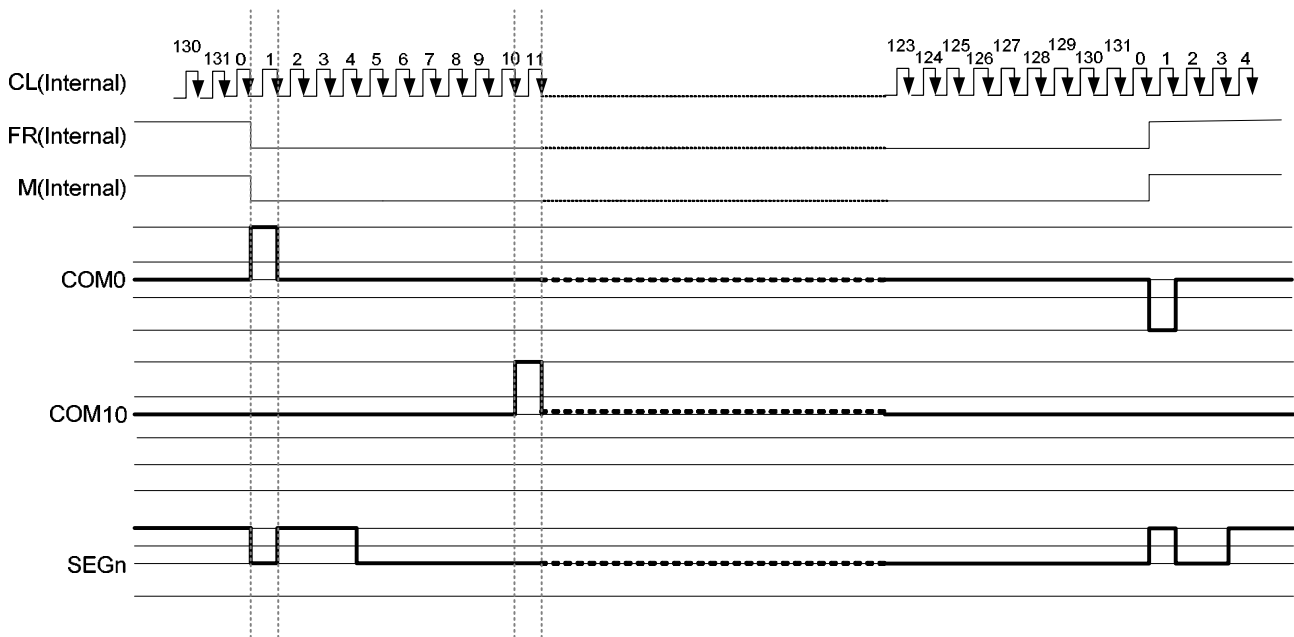


Figure 7.7-1 2-frame AC Driving Waveform (Duty Ratio: 1/132)

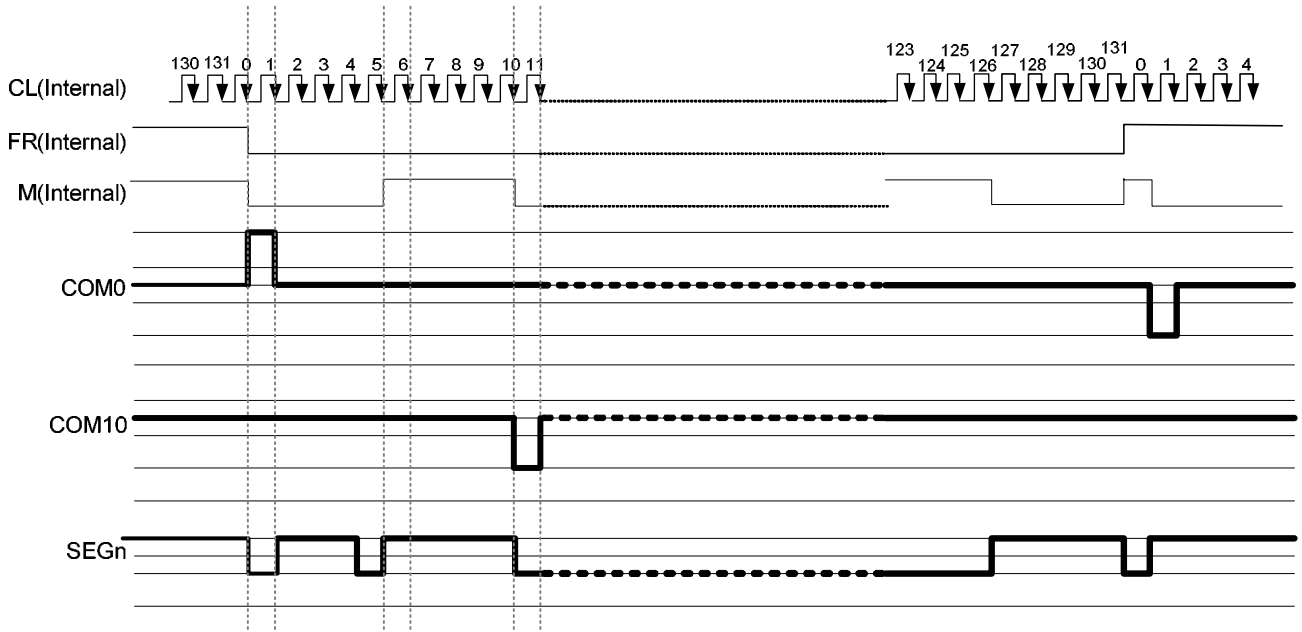


Figure 7.7-2 N-Line Inversion Driving Waveform (N=10, Duty Ratio=1/132)

7.8 POWER LEVEL DEFINITION

7.8.1. Power ON/OFF SEQUENCE

NOTE: VDDI=VDD, VDD1; VDDA=VDD2, VDD3, VDD4, VDD5

During power off, if LCD is in the Sleep Out mode, VDDA and VDDI must be powered down minimum 120msec after /RST has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDDA can be powered down minimum 0msec after /RST has been released.

/CS can be applied at any timing or can be permanently grounded. /RST has priority over /CS.

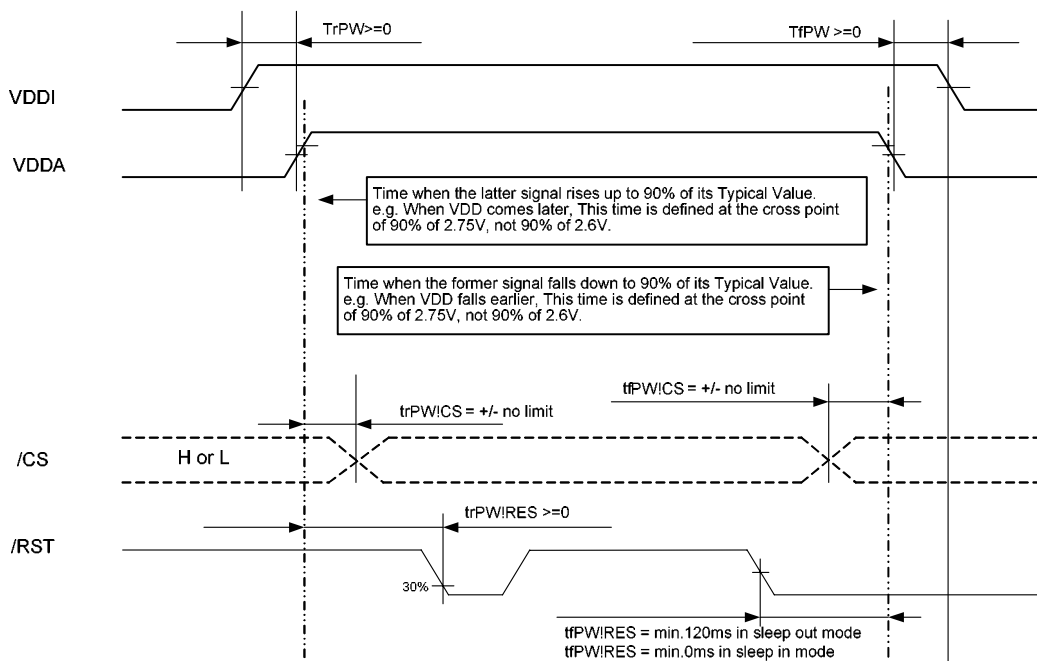
If /RST line is not held stable by host during Power On Sequence as defined in Sections case1 and case2, then it will be necessary to apply a Hardware Reset (/RST) after Host Power On Sequence is complete to ensure correct operation.

Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

Case 1 – /RST line is held High or Unstable by Host at Power On

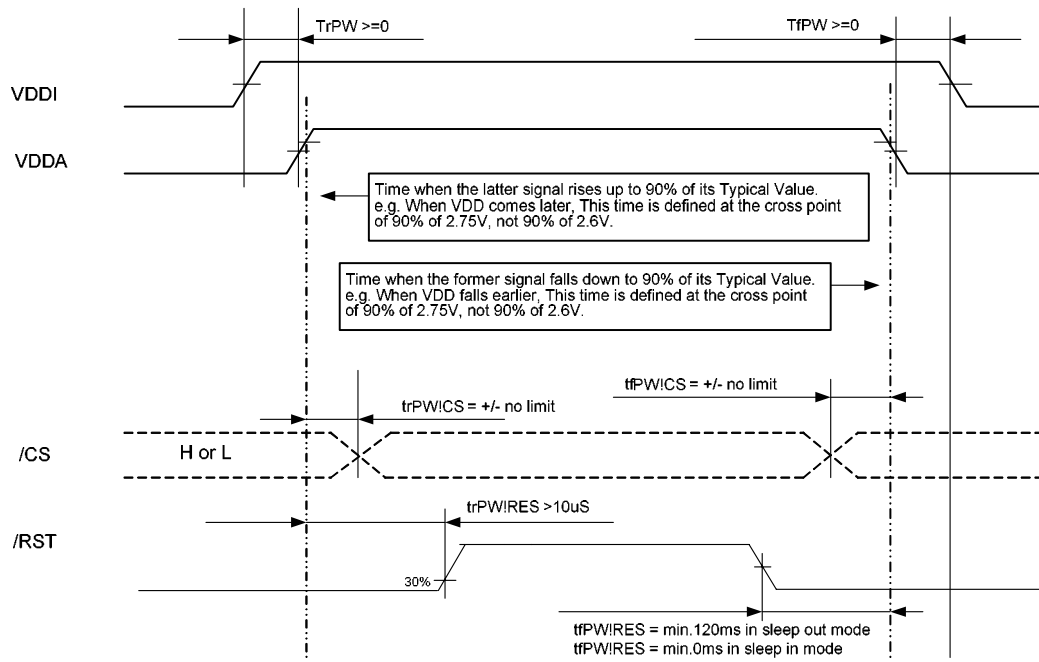
If /RST line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDDA and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Case 2 – /RST line is held Low by host at Power On

If /RST line is held Low (and stable) by the host during Power On, then the /RST must be held low for minimum 10μsec after both VDDA and VDDI have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.8.2. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out:

In this mode, the display is able to show maximum 65K colors.

2. Partial Mode On, Idle Mode Off, Sleep Out:

In this mode part of the display is used with maximum 65K colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out:

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out:

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode:

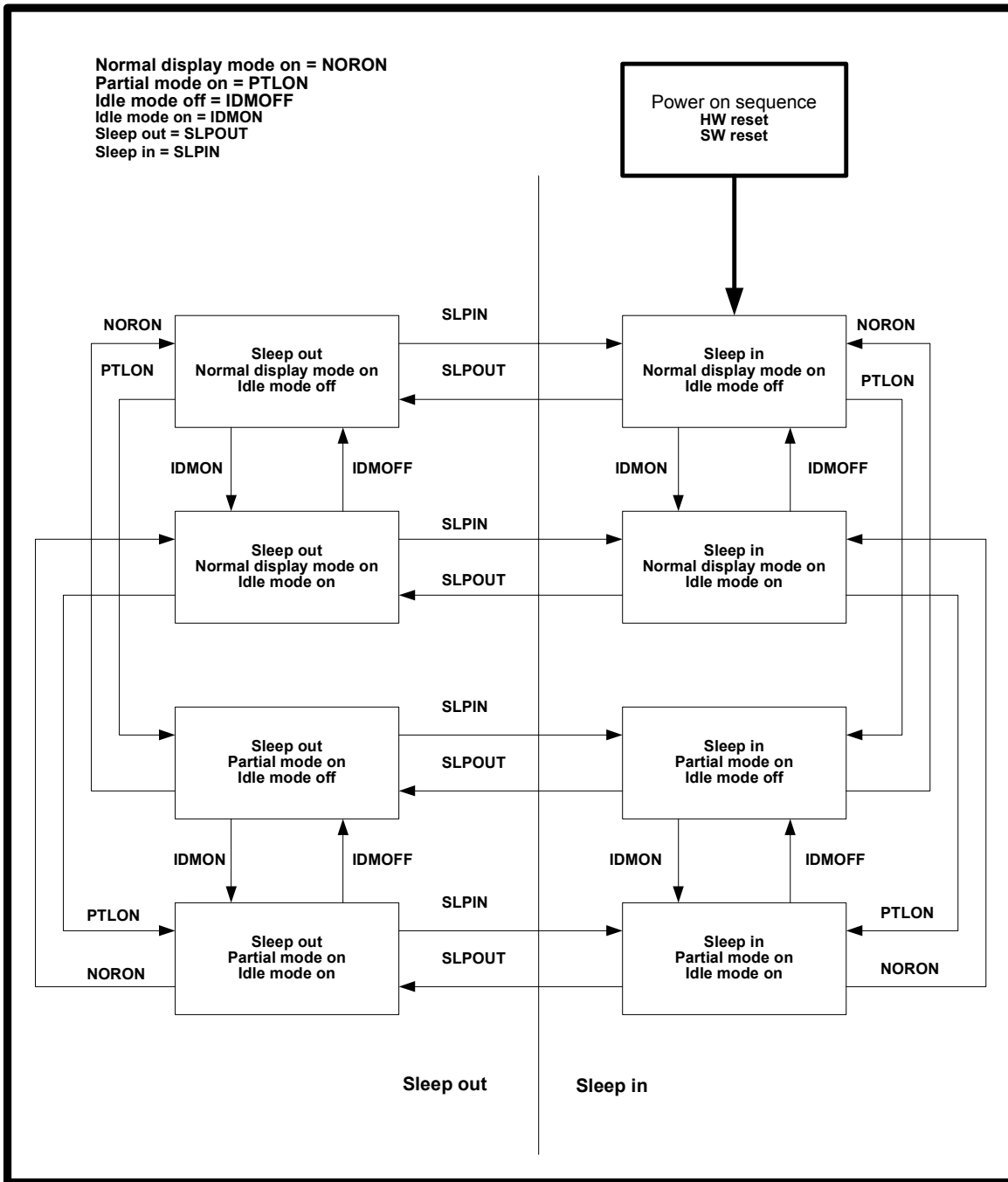
In this mode, the DC:DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with Digital VDD power supply. Contents of the memory are safe.

6. Power Off Mode:

In this mode, both Analog VDD and Digital VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

POWER FLOW CHART FOR DIFFERENT POWER MODES



Note

1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

7.9 Color Depth Conversion Look Up Table

R input (3bit) 256 colours 8 bit/pixel mode	R input (4bit) 4,096 colors 12 bit/pixel -mode	R input (5 bit) 65,536 colours 16 bit/pixel -mode	R output (6bit) 262,144 colours 18 bit/pixel -mode	RGBSET Parameter
000	0000	00000	R005 R004 R003 R002 R001 R000	1
001	0001	00001	R015 R014 R013 R012 R011 R010	2
010	0010	00010	R025 R024 R023 R022 R021 R020	3
011	0011	00011	R035 R034 R033 R032 R031 R030	4
100	0100	00100	R045 R044 R043 R042 R041 R040	5
101	0101	00101	R055 R054 R053 R052 R051 R050	6
110	0110	00110	R065 R064 R063 R062 R061 R060	7
111	0111	00111	R075 R074 R073 R072 R071 R070	8
Dummy Input	1000	01000	R085 R084 R083 R082 R081 R080	9
Dummy Input	1001	01001	R095 R094 R093 R092 R091 R090	10
Dummy Input	1010	01010	R105 R104 R103 R102 R127 R100	11
Dummy Input	1011	01011	R115 R114 R113 R112 R111 R110	12
Dummy Input	1100	01100	R125 R124 R123 R122 R121 R120	13
Dummy Input	1101	01101	R135 R134 R133 R132 R131 R130	14
Dummy Input	1110	01110	R145 R144 R143 R142 R141 R140	15
Dummy Input	1111	01111	R155 R154 R153 R152 R151 R150	16
Dummy Input	Dummy Input	10000	R165 R164 R163 R162 R161 R160	17
Dummy Input	Dummy Input	10001	R175 R174 R173 R172 R171 R170	18
Dummy Input	Dummy Input	10010	R185 R184 R183 R182 R181 R180	19
Dummy Input	Dummy Input	10011	R195 R194 R193 R192 R191 R190	20
Dummy Input	Dummy Input	10100	R205 R204 R203 R202 R201 R200	21
Dummy Input	Dummy Input	10101	R215 R214 R213 R212 R211 R210	22
Dummy Input	Dummy Input	10110	R225 R224 R223 R222 R221 R220	23
Dummy Input	Dummy Input	10111	R235 R234 R233 R232 R231 R230	24
Dummy Input	Dummy Input	11000	R245 R244 R243 R242 R241 R240	25
Dummy Input	Dummy Input	11001	R255 R254 R253 R252 R251 R250	26
Dummy Input	Dummy Input	11010	R265 R264 R263 R262 R261 R260	27
Dummy Input	Dummy Input	11011	R275 R274 R273 R272 R271 R270	28
Dummy Input	Dummy Input	11100	R285 R284 R283 R282 R281 R280	29
Dummy Input	Dummy Input	11101	R295 R294 R293 R292 R291 R290	30
Dummy Input	Dummy Input	11110	R305 R304 R303 R302 R301 R300	31
Dummy Input	Dummy Input	11111	R315 R314 R313 R312 R311 R310	32

ST7637

G input (3bit) 256 colours 8 bit/pixel mode	G input (4bit) 4,096 colors 12 bit/pixel -mode	G input (6 bit) 65,536 colours 16 bit/pixel -mode	G output (6bit) 262,144 colours 18 bit/pixel -mode	RGBSET Parameter
000	0000	000000	G005 G004 G003 G002 G001 G000	33
001	0001	000001	G015 G014 G013 G012 G011 G010	34
010	0010	000010	G025 G024 G023 G022 G021 G020	35
011	0011	000011	G035 G034 G033 G032 G031 G030	36
100	0100	000100	G045 G044 G043 G042 G041 G040	37
101	0101	000101	G055 G054 G053 G052 G051 G050	38
110	0110	000110	G065 G064 G063 G062 G061 G060	39
111	0111	000111	G075 G074 G073 G072 G071 G070	40
Dummy Input	1000	001000	G085 G084 G083 G082 G081 G080	41
Dummy Input	1001	001001	G095 G094 G093 G092 G091 G090	42
Dummy Input	1010	001010	G105 G104 G103 G102 G127 G100	43
Dummy Input	1011	001011	G115 G114 G113 G112 G111 G110	44
Dummy Input	1100	001100	G125 G124 G123 G122 G121 G120	45
Dummy Input	1101	001101	G135 G134 G133 G132 G131 G130	46
Dummy Input	1110	001110	G145 G144 G143 G142 G141 G140	47
Dummy Input	1111	001111	G155 G154 G153 G152 G151 G150	48
Dummy Input	Dummy Input	010000	G165 G164 G163 G162 G161 G160	49
Dummy Input	Dummy Input	010001	G175 G174 G173 G172 G171 G170	50
Dummy Input	Dummy Input	010010	G185 G184 G183 G182 G181 G180	51
Dummy Input	Dummy Input	010011	G195 G194 G193 G192 G191 G190	52
Dummy Input	Dummy Input	010100	G205 G204 G203 G202 G201 G200	53
Dummy Input	Dummy Input	010101	G215 G214 G213 G212 G211 G210	54
Dummy Input	Dummy Input	010110	G225 G224 G223 G222 G221 G220	55
Dummy Input	Dummy Input	010111	G235 G234 G233 G232 G231 G230	56
Dummy Input	Dummy Input	011000	G245 G244 G243 G242 G241 G240	57
Dummy Input	Dummy Input	011001	G255 G254 G253 G252 G251 G250	58
Dummy Input	Dummy Input	011010	G265 G264 G263 G262 G261 G260	59
Dummy Input	Dummy Input	011011	G275 G274 G273 G272 G271 G270	60
Dummy Input	Dummy Input	011100	G285 G284 G283 G282 G281 G280	61
Dummy Input	Dummy Input	011101	G295 G294 G293 G292 G291 G290	62
Dummy Input	Dummy Input	011110	G305 G304 G303 G302 G301 G300	63
Dummy Input	Dummy Input	011111	G315 G314 G313 G312 G311 G310	64
Dummy Input	Dummy Input	100000	G325 G324 G323 G322 G321 G320	65
Dummy Input	Dummy Input	100001	G335 G334 G333 G332 G331 G330	66

ST7637

Dummy Input	Dummy Input	100010	G345 G344 G343 G342 G341 G340	67
Dummy Input	Dummy Input	100011	G355 G354 G353 G352 G351 G350	68
Dummy Input	Dummy Input	100100	G365 G364 G363 G362 G361 G360	69
Dummy Input	Dummy Input	100101	G375 G374 G373 G372 G371 G370	70
Dummy Input	Dummy Input	100110	G385 G384 G383 G382 G381 G380	71
Dummy Input	Dummy Input	100111	G395 G394 G393 G392 G391 G390	72
Dummy Input	Dummy Input	101000	G405 G404 G403 G402 G401 G400	73
Dummy Input	Dummy Input	101001	G415 G414 G413 G412 G411 G410	74
Dummy Input	Dummy Input	101010	G425 G424 G423 G422 G421 G420	75
Dummy Input	Dummy Input	101011	G435 G434 G433 G432 G431 G430	76
Dummy Input	Dummy Input	101100	G445 G444 G443 G442 G441 G440	77
Dummy Input	Dummy Input	101101	G455 G454 G453 G452 G451 G450	78
Dummy Input	Dummy Input	101110	G465 G464 G463 G462 G461 G460	79
Dummy Input	Dummy Input	101111	G475 G474 G473 G472 G471 G470	80
Dummy Input	Dummy Input	110000	G485 G484 G483 G482 G481 G480	81
Dummy Input	Dummy Input	110001	G495 G494 G493 G492 G491 G490	82
Dummy Input	Dummy Input	110010	G505 G504 G503 G502 G501 G500	83
Dummy Input	Dummy Input	110011	G515 G514 G513 G512 G511 G510	84
Dummy Input	Dummy Input	110100	G525 G524 G523 G522 G521 G520	85
Dummy Input	Dummy Input	110101	G535 G534 G533 G532 G531 G530	86
Dummy Input	Dummy Input	110110	G545 G544 G543 G542 G541 G540	87
Dummy Input	Dummy Input	110111	G555 G554 G553 G552 G551 G550	88
Dummy Input	Dummy Input	111000	G565 G564 G563 G562 G561 G560	89
Dummy Input	Dummy Input	111001	G575 G574 G573 G572 G571 G570	90
Dummy Input	Dummy Input	111010	G585 G584 G583 G582 G581 G580	91
Dummy Input	Dummy Input	111011	G595 G594 G593 G592 G591 G590	92
Dummy Input	Dummy Input	111100	G605 G604 G603 G602 G601 G600	93
Dummy Input	Dummy Input	111101	G615 G614 G613 G612 G611 G610	94
Dummy Input	Dummy Input	111110	G625 G624 G623 G622 G621 G620	95
Dummy Input	Dummy Input	111111	G635 G634 G633 G632 G631 G630	96

ST7637

B input (3bit) 256 colours 8 bit/pixel mode	B input (4bit) 4,096 colors 12 bit/pixel -mode	B input (5 bit) 65,536 colours 16 bit/pixel -mode	B output (6bit) 262,144 colours 18 bit/pixel -mode	RGBSET Parameter
000	0000	00000	B005 B004 B003 B002 B001 B000	97
001	0001	00001	B015 B014 B013 B012 B011 B010	98
010	0010	00010	B025 B024 B023 B022 B021 B020	99
011	0011	00011	B035 B034 B033 B032 B031 B030	100
100	0100	00100	B045 B044 B043 B042 B041 B040	127
101	0101	00101	B055 B054 B053 B052 B051 B050	102
110	0110	00110	B065 B064 B063 B062 B061 B060	103
111	0111	00111	B075 B074 B073 B072 B071 B070	104
Dummy Input	1000	01000	B085 B084 B083 B082 B081 B080	105
Dummy Input	1001	01001	B095 B094 B093 B092 B091 B090	106
Dummy Input	1010	01010	B105 B104 B103 B102 B127 B100	107
Dummy Input	1011	01011	B115 B114 B113 B112 B111 B110	108
Dummy Input	1100	01100	B125 B124 B123 B122 B121 B120	109
Dummy Input	1101	01101	B135 B134 B133 B132 B131 B130	110
Dummy Input	1110	01110	B145 B144 B143 B142 B141 B140	111
Dummy Input	1111	01111	B155 B154 B153 B152 B151 B150	112
Dummy Input	Dummy Input	10000	B165 B164 B163 B162 B161 B160	113
Dummy Input	Dummy Input	10001	B175 B174 B173 B172 B171 B170	114
Dummy Input	Dummy Input	10010	B185 B184 B183 B182 B181 B180	115
Dummy Input	Dummy Input	10011	B195 B194 B193 B192 B191 B190	116
Dummy Input	Dummy Input	10100	B205 B204 B203 B202 B201 B200	117
Dummy Input	Dummy Input	10101	B215 B214 B213 B212 B211 B210	118
Dummy Input	Dummy Input	10110	B225 B224 B223 B222 B221 B220	119
Dummy Input	Dummy Input	10111	B235 B234 B233 B232 B231 B230	120
Dummy Input	Dummy Input	11000	B245 B244 B243 B242 B241 B240	121
Dummy Input	Dummy Input	11001	B255 B254 B253 B252 B251 B250	122
Dummy Input	Dummy Input	11010	B265 B264 B263 B262 B261 B260	123
Dummy Input	Dummy Input	11011	B275 B274 B273 B272 B271 B270	124
Dummy Input	Dummy Input	11100	B285 B284 B283 B282 B281 B280	125
Dummy Input	Dummy Input	11101	B295 B294 B293 B292 B291 B290	126
Dummy Input	Dummy Input	11110	B305 B304 B303 B302 B301 B300	127
Dummy Input	Dummy Input	11111	B315 B314 B313 B312 B311 B310	128

7.10 Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Figure 7.10-1 shows the referenced combinations in using Power Supply circuits.

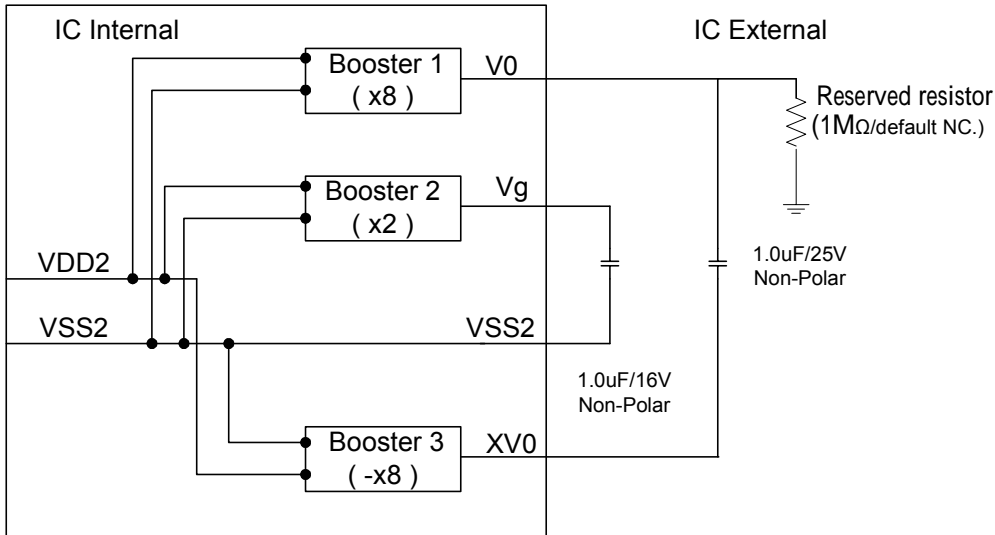


Figure 7.10-1 DC/DC Booster Block Diagram

7.10.1. Voltage Regulator Circuits

There is a built-in voltage regulator circuits in ST7637 for generating V0. After internal voltage is regulated by voltage regulator circuit, V0 is generated. Detail explanation of V0 set is listed below:

7.10.1.1. SET V0 (Temperatue = 24)

$$V0 = a + \{Vop[8:0] + Vop\text{-offset}[8:0] + (EV[6:0] - 3Fh)\} \times b \text{ (V)}$$

Example:

Vop[8:0]=011010010

Vop[8:0]=000000000

EV[6:0]=0111111

$V0 = 3.6 + \{ 210 + 0 + (63 - 63) \} \times 0.04 = 12 \text{ (V)}$

- a is a fixed constant value (see Table 7.10-2).
- b is a fixed constant value (see Table 7.10-2).
- Vop [8:0] is the programmed VOP value. The programming range for Vop[8:0] is 0 to 410 (19Ahex).
- The range of contrast is 128 steps for fine tuning VOP.

SYMBOL	VALUE	UNIT
a	3.6	V
b	0.04	V

Table 7.10-2

The Vop [8:0] value must be in the V0 programming range as given in Figure 7.10-3. Evaluating V0 equation, values outside the programming range indicated in many result. V0 range equals from 3.6V to 18V

$$(V0=3.6+\{vop[8:0]+vop\text{-offset}[8:0]+(EV[6:0]-3Fh)\}x0.04).$$

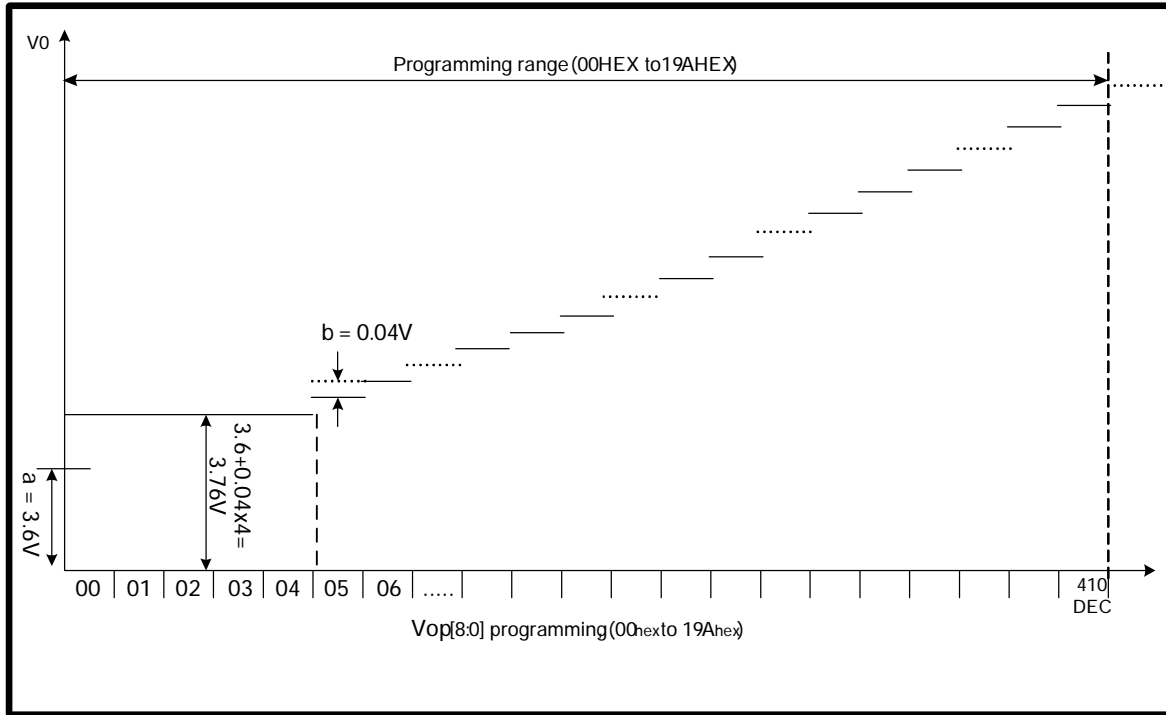


Figure 7.10-3 V0 programming range

As the programming range for the internally generated V0 voltage is above the limited V0 (18V), users has to ensure while selecting the temperature compensation that under all conditions and including all tolerances that the V0 voltage remains below 18V.

7.10.1.2. SET V0 with temperature compensation (Temperature ≠ 24)

There are 16-line slope in each temperature steps and customer can select one line slope of temperature compensation coefficient for each temperature step. Each temperature step is 8°C. Please see Figure 7.10-4 as below.

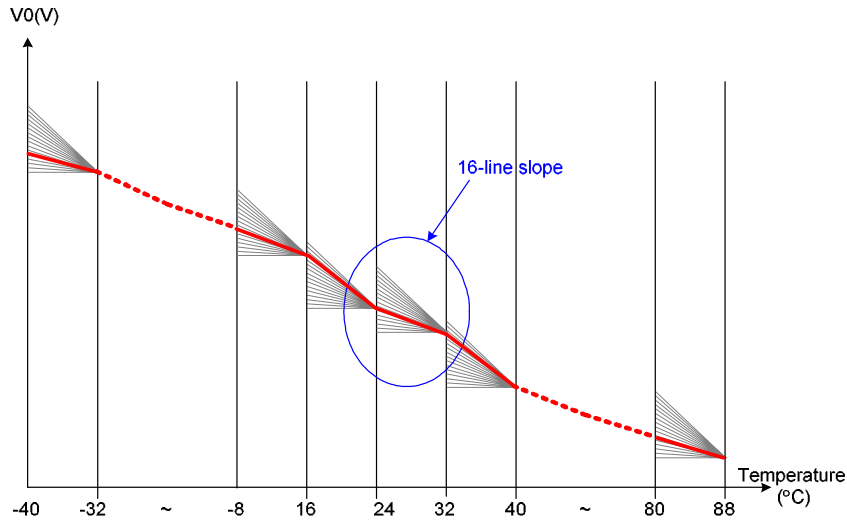
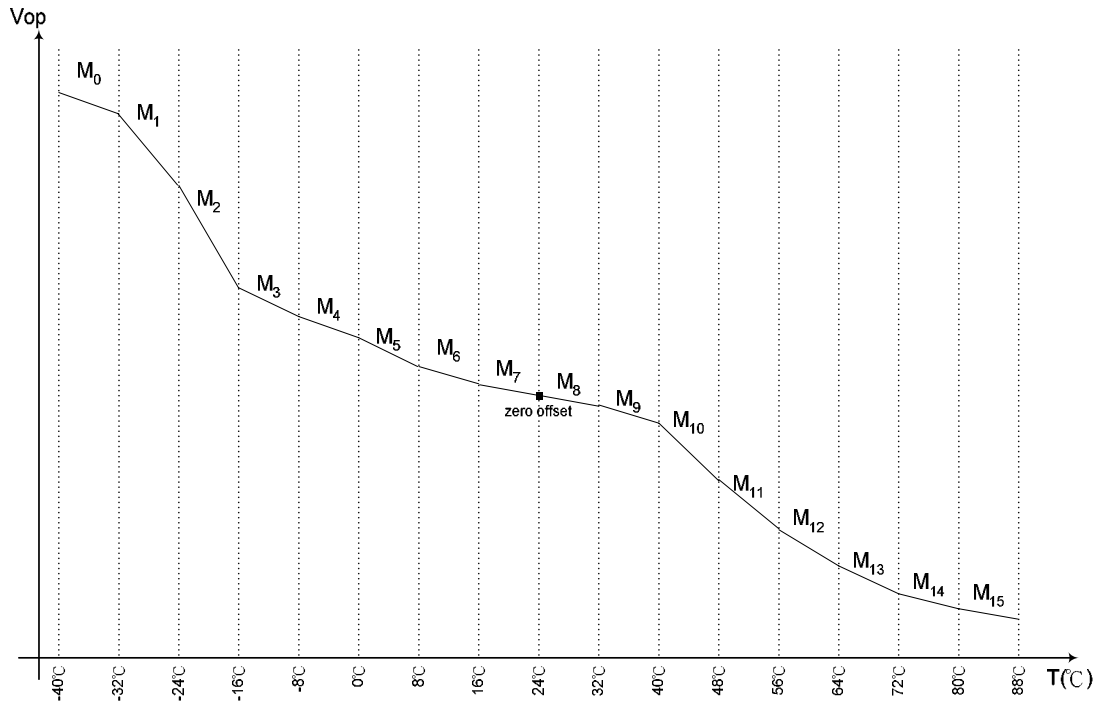


Figure 7.10-4

In command TEMPSEL (see section 9.1.72) each MT_x, where x=0, 1, 2,..., E, F, has a value between 0 and 15. MT_x = 0 results in 0V increment on V0, MT_x = 1 results in M_x=5mV increment, ..., MT_x = 15 results in M_x=15x5mV=75mV increment. Note that each MT_x individually corresponds to a temperature interval; The relations between M_x and V0 quantity due to temperature V0(T) are described in the equations shown as follows:

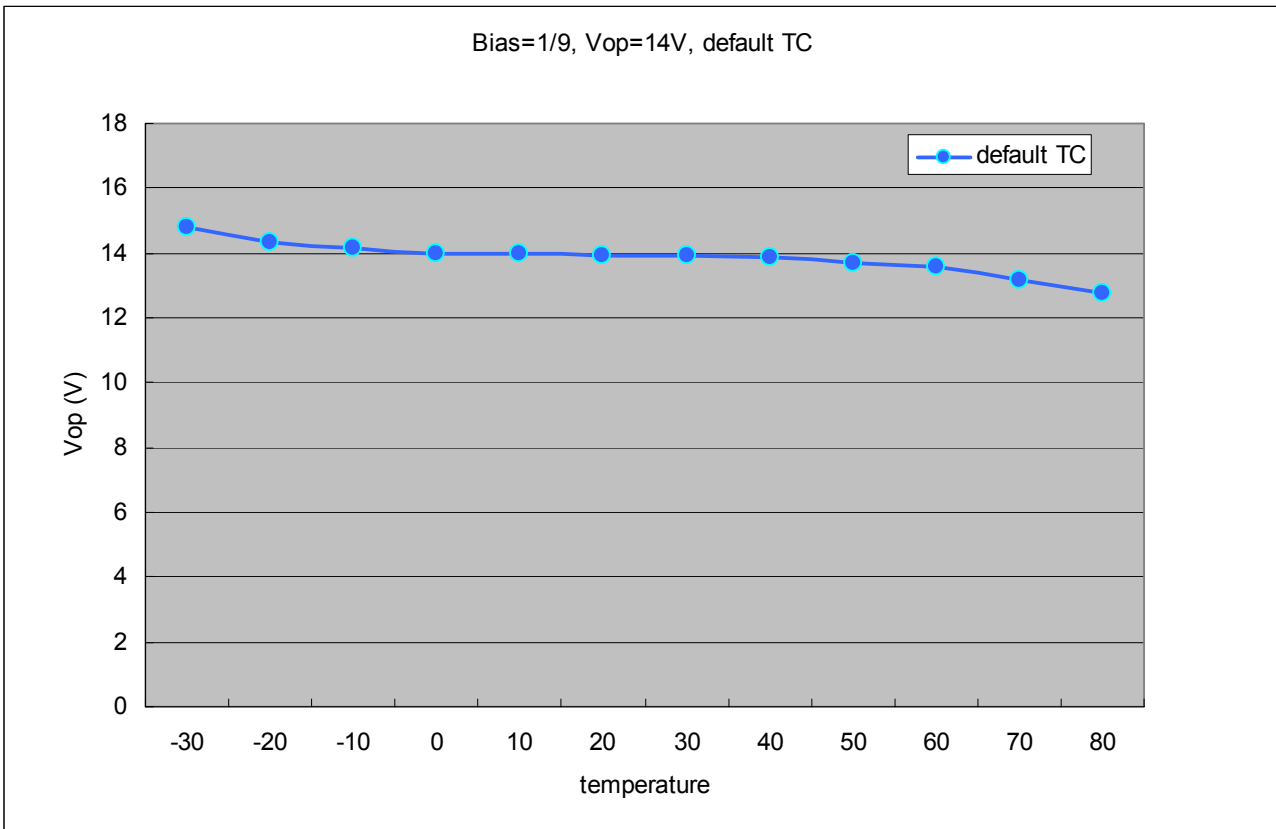
Temperature range	Equation V0(V) at temperature=T
-40 T < -32	$V0(T) = V0(T_{24}) + (-32-T) \cdot M0 + (M1 + M2 + M3 + M4 + M5 + M6 + M7) \cdot 8$
-32 T < -24	$V0(T) = V0(T_{24}) + (-24-T) \cdot M1 + (M2 + M3 + M4 + M5 + M6 + M7) \cdot 8$
-24 T < -16	$V0(T) = V0(T_{24}) + (-16-T) \cdot M2 + (M3 + M4 + M5 + M6 + M7) \cdot 8$
-16 T < -8	$V0(T) = V0(T_{24}) + (-8-T) \cdot M3 + (M4 + M5 + M6 + M7) \cdot 8$
-8 T < 0	$V0(T) = V0(T_{24}) + (0-T) \cdot M4 + (M5 + M6 + M7) \cdot 8$
0 T < 8	$V0(T) = V0(T_{24}) + (8-T) \cdot M5 + (M6 + M7) \cdot 8$
8 T < 16	$V0(T) = V0(T_{24}) + (16-T) \cdot M6 + M7 \cdot 8$
16 T < 24	$V0(T) = V0(T_{24}) + (24-T) \cdot M7$
24 T < 32	$V0(T) = V0(T_{24}) - (T-24) \cdot M8$
32 T < 40	$V0(T) = V0(T_{24}) - (T-32) \cdot M9 - M8 \cdot 8$
40 T < 48	$V0(T) = V0(T_{24}) - (T-40) \cdot M10 - (M9 + M8) \cdot 8$
48 T < 56	$V0(T) = V0(T_{24}) - (T-48) \cdot M11 - (M10 + M9 + M8) \cdot 8$
56 T < 64	$V0(T) = V0(T_{24}) - (T-56) \cdot M12 - (M11 + M10 + M9 + M8) \cdot 8$
64 T < 72	$V0(T) = V0(T_{24}) - (T-64) \cdot M13 - (M12 + M11 + M10 + M9 + M8) \cdot 8$
72 T < 80	$V0(T) = V0(T_{24}) - (T-72) \cdot M14 - (M13 + M12 + M11 + M10 + M9 + M8) \cdot 8$
80 T < 88	$V0(T) = V0(T_{24}) - (T-80) \cdot M15 - (M14 + M13 + M12 + M11 + M10 + M9 + M8) \cdot 8$



ST7637

Setting example for default TC curve

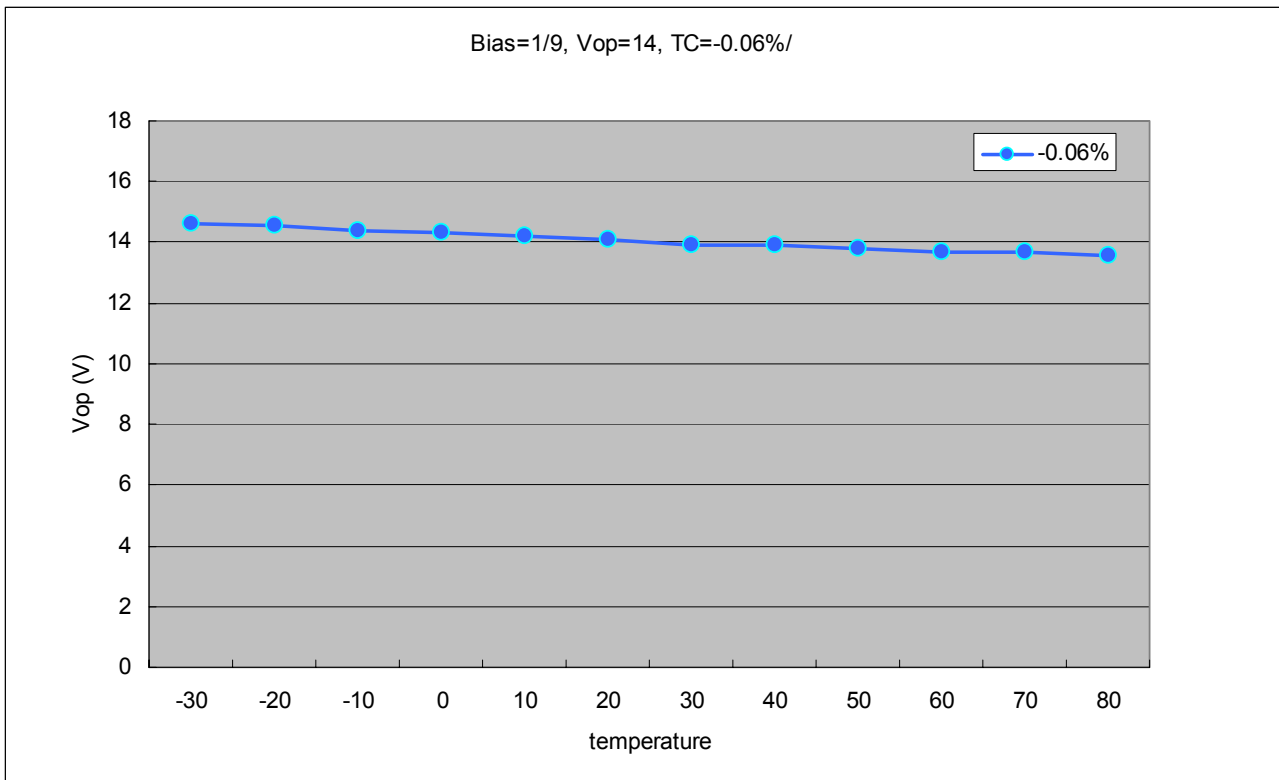
COMMAND	
0xF4	
DATA	
1 st : 0xFF	2 nd : 0x36
3 rd : 0x04	4 th : 0x00
5 th : 0x33	6 th : 0x42
7 th : 0xC4	8 th : 0x59



ST7637

Setting example for TC curve=-0.06%/

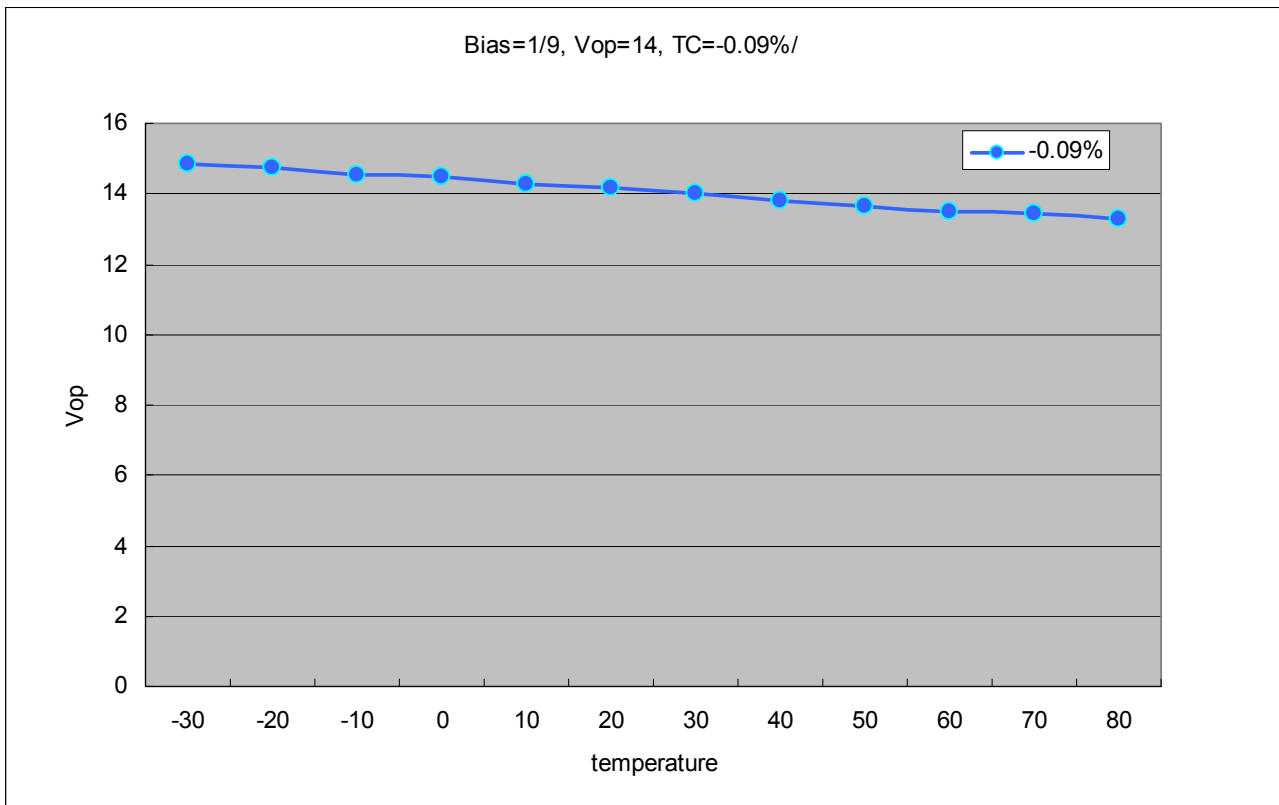
COMMAND	
0xF4	
DATA	
1 st : 0x33	2 nd : 0x33
3 rd : 0x33	4 th : 0x33
5 th : 0x33	6 th : 0x33
7 th : 0x33	8 th : 0x33



ST7637

Setting example for TC curve=-0.09%/

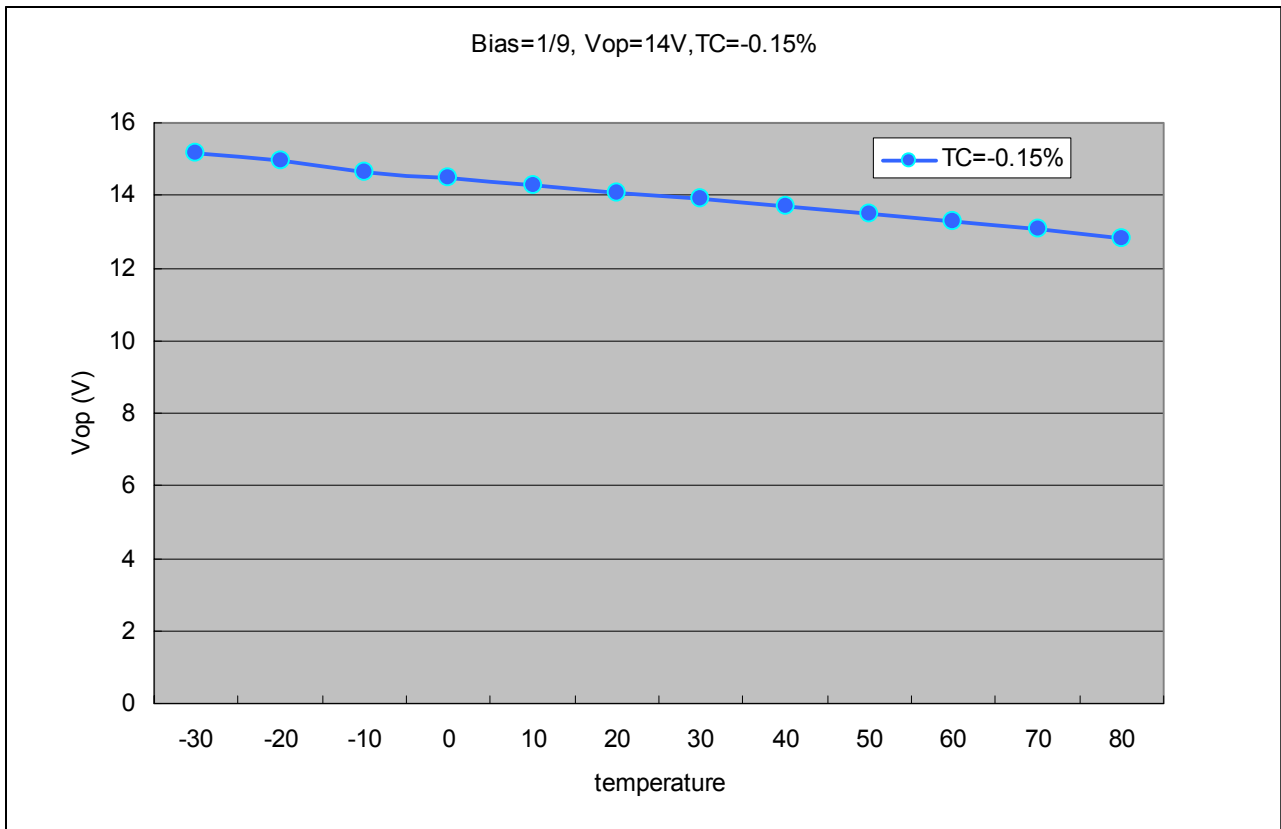
COMMAND	
0xF4	
DATA	
1 st : 0x44	2 nd : 0x44
3 rd : 0x44	4 th : 0x44
5 th : 0x44	6 th : 0x44
7 th : 0x44	8 th : 0x44



ST7637

Setting example for TC curve=-0.15%/

COMMAND	
0xF4	
DATA	
1 st : 0x55	2 nd : 0x55
3 rd : 0x55	4 th : 0x55
5 th : 0x55	6 th : 0x55
7 th : 0x55	8 th : 0x55



7.10.1.3. V0 fine tuning

ST7637 has 2 commands for fine tuning V0. These commands are VopOffsetInc (see section 9.1.47) and VopOffsetDec (see section 9.1.48). When writing VopOffsetInc into IC for each time, V0 would increase 40mV; when writing VopOffsetDec into IC for each time, V0 would decrease 40mV.

Example:

Vop[8:0]=011010010

EV[6:0]=0111111

VopOffsetInc x2

→ $V0 = 3.6 + \{ 210 + (63-63) \} \times 0.04 + 0.04 \times 2 = 12.08 \text{ (V)}$

7.10.2. Voltage Follower Circuits

There is a build-in voltage follower circuits in ST7637 for generating Vg and Vm. These voltages are decided by bias ratio selection circuitry which is set by users with software to control 1/5 to 1/12 bias ratios to match the optimum display performance of LCD panel. Bias driving rule is listed below:

LCD bias	Vg	Vm
1/N bias	$(2/N) \times V0$	$(1/N) \times V0$

N=5 to 12

7.10.3. OTP Setting Flow

ST7637 provides the Write and Read function to write the electronic control value and built-in resistance ratio into built-in OTP, and then read them from it. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attention the setting procedure. Please see the following diagram.

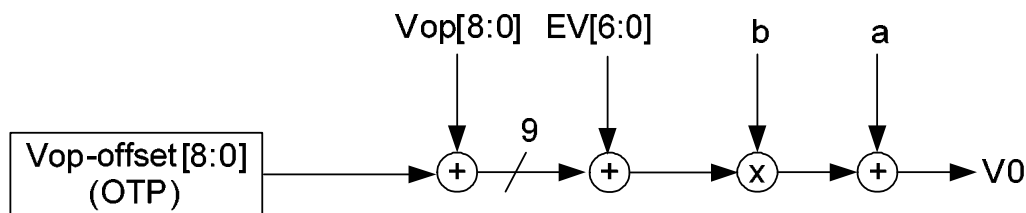


Figure 7.10-5 V0 value control for different modules by loading OTP offset

Note1: This setting flow is used for LCM assembler.

Note2: OTP shouldn't be written without preceding loading correctly from OTP in order to avoid some errors during IC operation.

Note3: When writing value to OTP, the voltage of VPP must be more than 7.5V (7.5V~7.75V); the current of Ivpp must be more than 4 mA.

Note4: If the OTP is exposed to a high temperature for hours, data in the memory cell may probably be lost before the data retention guarantee period. To retain data in the memory cell, keep the memory cell below 90 . The data retention guarantee period is specified including the retention period.

7.11 Frquency Temperature Gradient Compensation Coefficient

ST7637 will auto-switch frame rate on different temperature such as Figure 7.11-1. TA, TB and TC are frame rate switching temperatures which can be defined by customer with command TMPRNG(see section 9.1.70). FA, FB, FC and FD are switched frame rate which also can be defined by customer with command FRMSEL (see section 9.1.65). The frame rate range is from 37.5Hz to 170Hz.

When the temperature is in increasing state, frame rate changes to the higher step at TA/TB/TC+TH(). When the temperature is in decreasing state, frame rate changes to the lower step at TA/TB/TC. For example: TC=10 and TH=5 , FC switches to FD at 15 but FD switches to FC at 10 . Please take Figure 7.11-1 for reference.

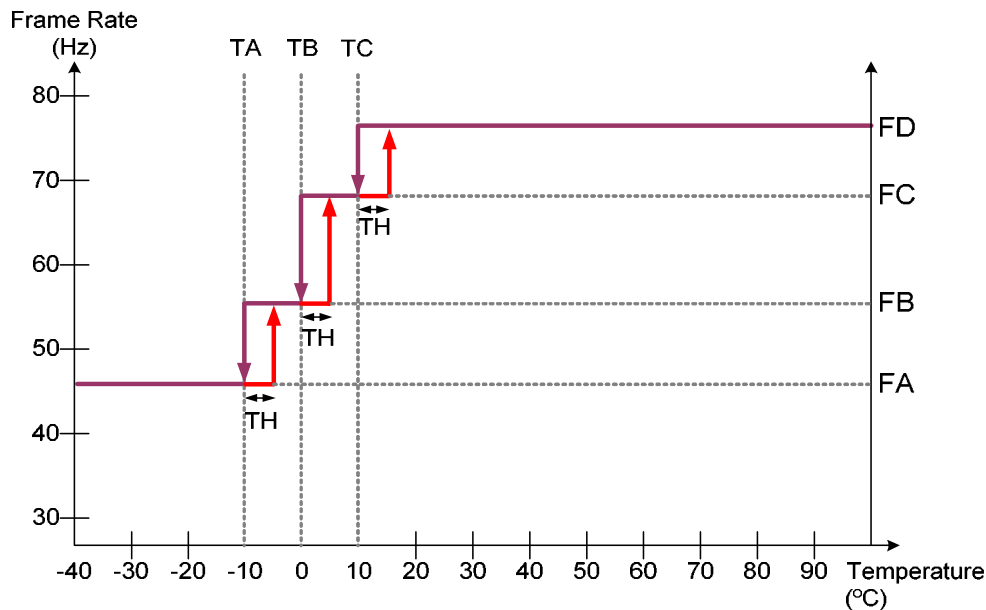


Figure 7.11-1

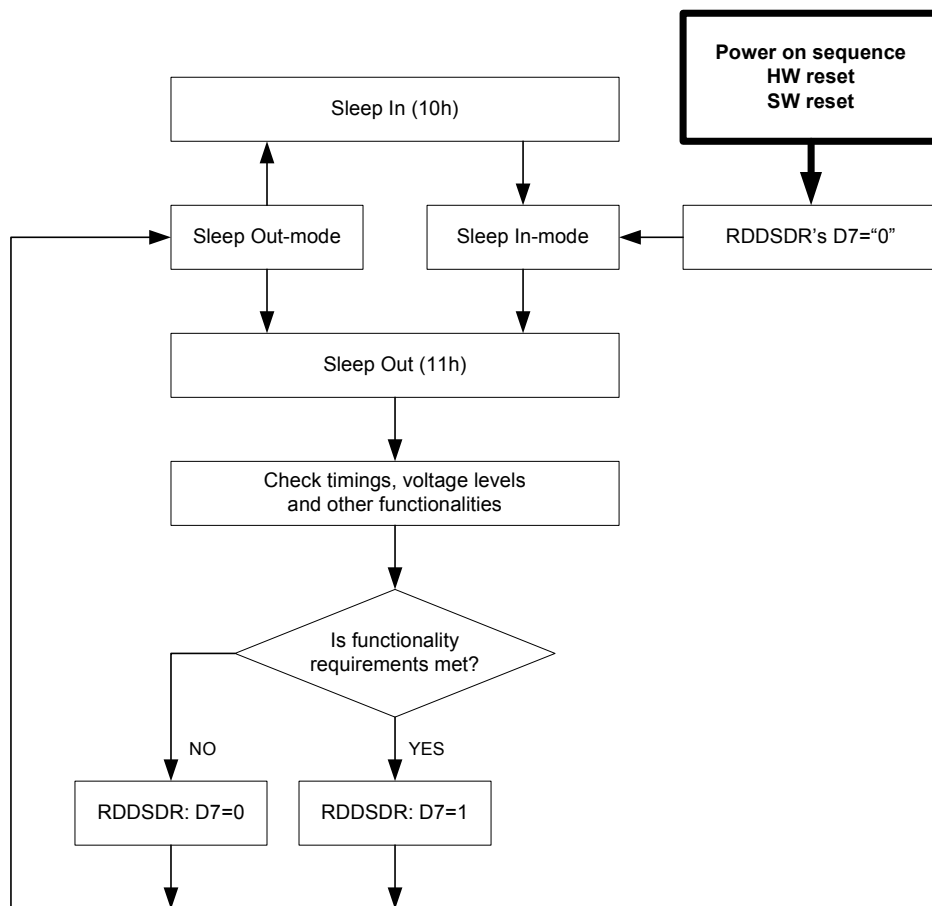
7.12 Sleep Out –Command and Self-Diagnostic Functions of the Display Module

7.12.1. Register loading Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP ROM to registers of the display controller is working properly.

There are compared factory values of the OTP ROM and register values of the display controller by the display controller (1st step: compare register and OTP ROM values, 2nd step: loads OTP ROM values to registers). If those both values (OTP ROM and register values) are same, bit-7 of RDDSDR is set to 1, which is defined in command RDDSDR (The used bit of this command is D7). If those both values are not same, this bit (D7) is set to 0.

The flow chart for this internal function is following:

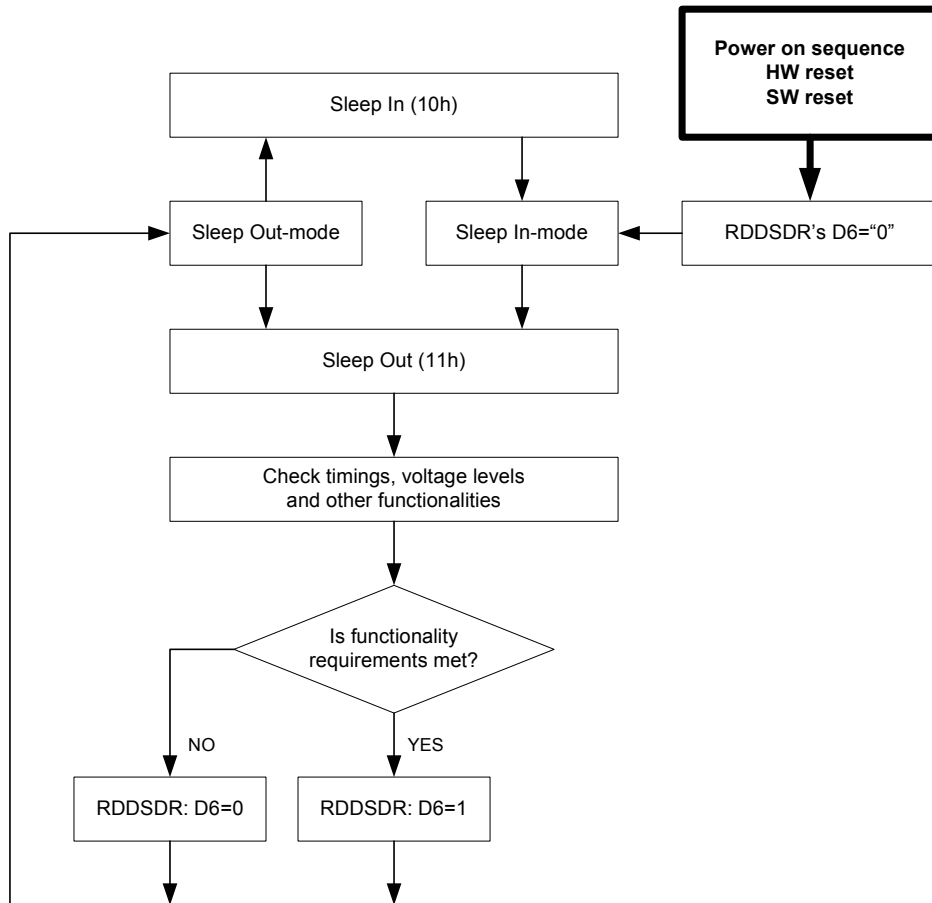


7.12.2. Functionality Detection

Sleep Out-command is a trigger for an internal function of the display module.

The internal function (= the display controller) is comparing if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, bit-6 of RDDSDR is set to 1, which defined in command Read Display Self-Diagnostic Result (RDDSDR). The used bit of this command is D6. If functionality requirement is not same, this bit (D6) is set to 0.

The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In -mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid.

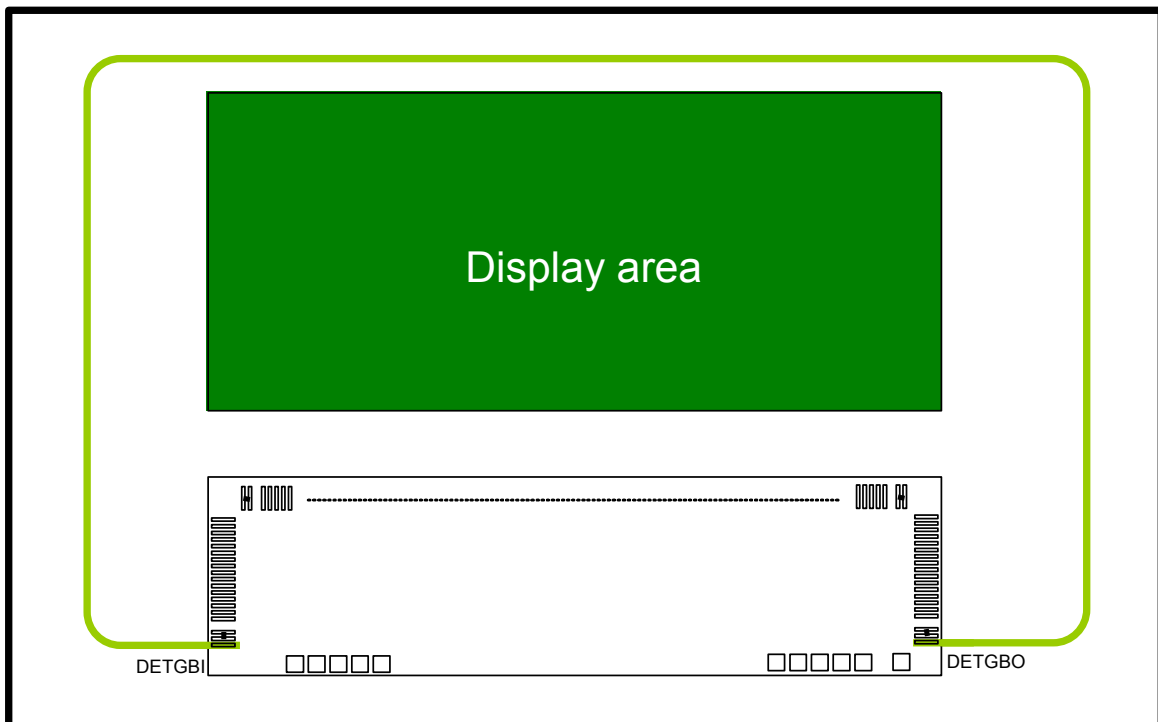
Otherwise, there is 5msec delay for D6's value, when Sleep Out -command is sent in Sleep Out -mode.

7.12.3. LCM Glass Detection (Function Reserved)

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display glass of the display module is broken or not.

This feature uses bit-4 (D4) in the parameter of command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) as the indicator. If this display glass is broken, this bit (D4) is set to 0.

The following figure is a reference of how this glass break detection can be implemented. For example, there is connected together 2 bumps (DETGBI and DETGBO) via route of ITO. This route of ITO is the nearest route of the edge of the display glass.



8. RESET CIRCUIT

The registers that are initialized are listed below.

Item	After Power On	After Software Reset	After Hardware Reset
Frame memory (RAM data)	Random	No Change	No Change
RDDID	TBD	TBD	TBD
RDDPM	08h	08h	08h
RDDMADCTR	00h	No Change	00h
RDDCOLMOD	05h (16-Bit/Pixel)	No Change	05h (16-Bit/Pixel)
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
Sleep In/Out	In	In	In
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
All Pixel Off mode	Disable	Disable	Disable
All Pixel On mode	Disable	Disable	Disable
Contrast (EV)	3Fh	3Fh	3Fh
Display On/Off	Display Off	Display Off	Display Off
Column: Start Address (XS)	00h	00h	00h
Column: End Address (XE)	83h	83h (when MV=0) 83h (when MV=1)	83h
Row: Start Address (YS)	00h	00h	00h
Row: End Address (YE)	83h	83h (when MV=0) 83h (when MV=1)	83h
Color set	Random	Contents of the look-up table protected	Random
Partial: Start Address (PS)	00h	00h	00h
Partial: End Address (PE)	83h	83h	83h
Scroll: Top Fixed Area (TFA)	00h	00h	00h
Scroll: Scroll Area (VSA)	84h	84h	84h
Scroll: Bottom Fixed Area (BFA)	00h	00h	00h
TE On/Off	Off	Off	Off
TE Mode	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control MY/MX/MV/ML/RGB)	0/0/0/0/0	No Change	0/0/0/0/0
Scroll Start Address (SSA)	00h	00h	00h
Idle Mode On/Off	Off	Off	Off
Interface Color Pixel Format (P)	05h (16Bit/Pixel)	No change	05h (16Bit/Pixel)
ID1	Set by customer	Set by customer	Set by customer
ID2	Set by customer	Set by customer	Set by customer
ID3	Set by customer	Set by customer	Set by customer
Drive Duty	83h	83h	83h
First Common	00h	00h	00h
FOSC Divider	No division	No division	No division
Common scan direction	0→65, 66→131	0→65, 66→131	0→65, 66→131

Item	After Power On	After Software Reset	After Hardware Reset
Vop	0D2h	0D2h	0D2h
Vop Offset increase/decrease	disable	disable	disable
Bias	1/6 Bias	1/6 Bias	1/6 Bias
Booster setting	7x	7x	7x
Booster Efficiency	01	01	01
Vg source	From 2VDD2	From 2VDD2	From 2VDD2
EPCTIN	0	0	0
OTP selection	Disable	Disable	Disable
Frame Frequency in Normal Color (FA/FB/FC/FD)	46Hz/61.5Hz/72Hz/77Hz	46Hz/61.5Hz/72Hz/77Hz	46Hz/61.5Hz/72Hz/77Hz
Frame Frequency in 8-Color (Idle) (F8A/F8B/F8C/F8D)	46Hz/61.5Hz/72Hz/77Hz	46Hz/61.5Hz/72Hz/77Hz	46Hz/61.5Hz/72Hz/77Hz
Temperature Range (TA/TB/TC)	-10 /0 /10	-10 /0 /10	-10 /0 /10
Temperature Hysteresis (TH)	6	6	6
TEMPSEL	Refer to 9.1.72	Refer to 9.1.72	Refer to 9.1.72

9. INSTRUCTIONS

9.1 Instruction table

Command Table-1 , /EXT= H , L, or floating														
Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(00h)	NOP	0	1	0	0	0	0	0	0	0	0	0	No Operation	9.1.1
(01h)	SWRESET	0	1	0	0	0	0	0	0	0	0	1	Software reset	9.1.2
(04h)	RDDID	0	1	0	0	0	0	0	0	1	0	0	Read Display ID	9.1.3
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	ID1 read (D23-D16)	
-		1	0	1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	ID2 read (D15-D8)	
-		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	ID3 read (D7-D0)	
(09h)	RDDST	0	1	0	0	0	0	0	1	0	0	1	Read Display Status	9.1.4
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	(D31-D24)	
-		1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	(D23-D16)	
-		1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	(D15-D8)	
-		1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	(D7-D0)	
(0Ah)	RDDPM	0	1	0	0	0	0	0	1	0	1	0	Read Display Power Mode	9.1.5
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	D2	0	0	-	
(0Bh)	RDDMADCTR	0	1	0	0	0	0	0	1	0	1	1	Read Display MADCTR	9.1.6
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	0	0	0	-	
(0Ch)	RDDCOLMOD	0	1	0	0	0	0	0	1	1	0	0	Read Display Pixel Format	9.1.7
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	0	0	0	0	0	D2	D1	D0	-	
(0Dh)	RDDIM	0	1	0	0	0	0	0	1	1	0	1	Read Display Image Mode	9.1.8
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	0	D5	D4	D3	0	0	0	-	
(0Eh)	RDDSM	0	1	0	0	0	0	0	1	1	1	0	Read Display Image Mode	9.1.9
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	0	0	0	0	0	0	-	
(0Fh)	RDDSDR	0	1	0	0	0	0	0	1	1	1	1	Read Display Self-diagnostic result	9.1.10
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	0	D4	0	0	0	0	-	

ST7637

(10h)	SLPIN	0	1	0	0	0	0	1	0	0	0	0	Sleep in & booster off	9.1.11
(11h)	SLPOUT	0	1	0	0	0	0	1	0	0	0	1	Sleep out & booster on	9.1.12
(12h)	PTLON	0	1	0	0	0	0	1	0	0	1	0	Partial mode on	9.1.13
(13h)	NORON	0	1	0	0	0	0	1	0	0	1	1	Partial off (Normal)	9.1.14
(20h)	INVOFF	0	1	0	0	0	1	0	0	0	0	0	Display inversion off (normal)	9.1.15
(21h)	INVON	0	1	0	0	0	1	0	0	0	0	1	Display inversion on	9.1.16
(22h)	APOFF	0	1	0	0	0	1	0	0	0	1	0	All pixel off (Only for test purpose)	9.1.17
(23h)	APON	0	1	0	0	0	1	0	0	0	1	1	All pixel on (Only for test purpose)	9.1.18
(25h)	WRCNTR	0	1	0	0	0	1	0	0	1	0	1	Write contrast	9.1.19
-		1	1	0	0	EV6	EV5	EV4	EV3	EV2	EV1	EV0	EV = 0 to 127	
(28h)	DISPOFF	0	1	0	0	0	1	0	1	0	0	0	Display off	9.1.20
(29h)	DISPON	0	1	0	0	0	1	0	1	0	0	1	Display on	9.1.21
(2Ah)	CASET	0	1	0	0	0	1	0	1	0	1	0	Column address set	9.1.22
		1	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	X_ADR start: 0 XS 83h	
		1	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	X_ADR end: XS XE 83h	
(2Bh)	RASET	0	1	0	0	0	1	0	1	0	1	1	Row address set	9.1.23
		1	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	Y_ADR start: 0 YS 83h	
		1	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	Y_ADR end: YS YE 83h	
(2Ch)	RAMWR	0	1	0	0	0	1	0	1	1	0	0	Memory write	9.1.24
		1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data	
(2Dh)	RGBSET	0	1	0	0	0	1	0	1	1	0	1	Color set for 256 or 4k color display	9.1.25
-		1	1	0	-	-	-	R4	R3	R2	R1	R0	Red tone (00000)	
-		1	1	0	:	:	:	:	:	:	:	:	:-	
-		1	1	0	-	-	-	R4	R3	R2	R1	R0	Red tone (11111)	
-		1	1	0	-	-	G5	G4	G3	G2	G1	G0	Green tone (000000)	
		1	1	0	:	:	:	:	:	:	:	:	:-	
		1	1	0	-	-	G5	G4	G3	G2	G1	G0	Green tone (111111)	
		1	1	0	-	-	-	B4	B3	B2	B1	B0	Blue tone (00000)	
		1	1	0	:	:	:	:	:	:	:	:	:-	
		1	1	0	-	-	-	B4	B3	B2	B1	B0	Blue tone (11111)	
(2Eh)	RAMRD	0	1	0	0	0	1	0	1	1	1	0	Memory Read	9.1.26
		1	1	0	-	-	-	-	-	-	-	-	Dummy read	
		1	1	0	D7	D6	D5	D4	D3	D2	D1	D0		
(30h)	PTLAR	0	1	0	0	0	1	1	0	0	0	0	Partial start/end address set	9.1.27

ST7637

-		1	1	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	Start address (0~131)	
-		1	1	0	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	End address (0~131)	
(33h)	SCRLAR	0	1	0	0	0	1	1	0	0	1	1	Scroll Area	9.1.28
-		1	1	0	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	TFA=0~132	
-		1	1	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	VSA=0~132	
-		1	1	0	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	BFA=0~132	
(34h)	TEOFF	0	1	0	0	0	1	1	0	1	0	0	Tearing effect line off	9.1.29
(35h)	TEON	0	1	0	0	0	1	1	0	1	0	1	Tearing effect mode set & on	9.1.30
-		1	1	0	-	-	-	-	-	-	-	M	"0": mode1, "1": mode2	
(36h)	MADCTR	0	1	0	0	0	1	1	0	1	1	0	Memory data access control	9.1.31
-		1	1	0	MY	MX	MV	ML	RGB	-	-	-	-	
(37h)	VSCSAD	0	1	0	0	0	1	1	0	1	1	1	Scroll start address of RAM	9.1.32
		1	1	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	SSA = 0~131	
(38h)	IDMOFF	0	1	0	0	0	1	1	1	0	0	0	Idle mode off	9.1.33
(39h)	IDMON	0	1	0	0	0	1	1	1	0	0	1	Idle mode on	9.1.34
(3Ah)	COLMOD	0	1	0	0	0	1	1	1	0	1	0	Interface pixel format	9.1.35
-		1	1	0	-	-	-	-	-	P2	P1	P0	Interface format	
(DAh)	RDID1	0	1	0	1	1	0	1	1	0	1	0	Read ID1	9.1.36
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	(D7-D0)	
(DBh)	RDID2	0	1	0	1	1	0	1	1	0	1	1	Read ID2	9.1.37
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	(D7-D0)	
(DCh)	RDID3	0	1	0	1	1	0	1	1	1	0	0	Read ID3	9.1.38
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	(D7-D0)	

Note 1: When /EXT connects to H or floating, commands which are not defined in "Command Table-1" are treated as NOP (00H) command.

Note 2: Commands 10H, 12H, 13H, 20H, 21H, 25H, 28H, 29H, 30H, 36H (Bit ML only), 38H and 39H are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects.

During Sleep In mode, these commands are updated immediately.

Read status (09H), Read Display Power Mode (0AH), Read Display MADCTR (0BH), Read Display Pixel Format (0CH), Read Display Image Mode (0DH), Read Display Signal Mode (0EH) and Read Display Self Diagnostic Result (0FH) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

Command Table-2 , /EXT= L or command D7h[7] enable														
Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(B0h)	DutySet	0	1	0	1	0	1	1	0	0	0	0	Display Duty setting	9.1.39
		1	1	0	Du7	Du6	Du5	Du4	Du3	Du2	Du1	Du0		
(B1h)	FirstCom	0	1	0	1	0	1	1	0	0	0	1	First Com. Page address	9.1.40
		1	1	0	--	F6	F5	F4	F3	F2	F1	F0		
(B3h)	OscDiv	0	1	0	1	0	1	1	0	0	1	1	FOSC divider	9.1.41
		1	1	0	-	-	-	-	-	-	CLD1	CLD0		
(B5h)	NLInvSet	0	1	0	1	0	1	1	0	1	0	1	N-line control	9.1.42
		1	1	0	M	N6	N5	N4	N3	N2	N1	N0		
(B7h)	ComScanDir	0	1	0	1	0	1	1	0	1	1	1	Com/Seg Scan Direction for Glass layout	9.1.43
		1	1	0	0	SMX	0	0	SBGR	0	0	0		
(B8h)	RmwIn	0	1	0	1	0	1	1	1	0	0	0	read modify write control IN	9.1.44
(B9h)	RmwOut	0	1	0	1	0	1	1	1	0	0	1	read modify write control Out	9.1.45
(C0h)	VopSet	0	1	0	1	1	0	0	0	0	0	0	Vop setting	9.1.46
		1	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0		
		1	1	0	-	-	-	-	-	-	-	Vop8		
(C1h)	VopOfsetInc	0	1	0	1	1	0	0	0	0	0	1	+40mv/setp	9.1.47
(C2h)	VopOfsetDec	0	1	0	1	1	0	0	0	0	1	0	-40mv/setp	9.1.48
(C3h)	BiasSel	0	1	0	1	1	0	0	0	0	1	1	Bias selection	9.1.49
		1	1	0	-	-	-	-	-	Bias2	Bias1	Bias0		
(C4h)	BstBmpXSel	0	1	0	1	1	0	0	0	1	0	0	Booster setting	9.1.50
		1	1	0	-	-	-	-	-	BST2	BST 1	BST0		
(C5h)	BstEffSel	0	1	0	1	1	0	0	0	1	0	1	Booster efficiency selection	9.1.51
		1	1	0	-	-	-	-	-	-	BTF1	BTF0		
(C7h)	VopOffset	0	1	0	1	1	0	0	0	1	1	1		9.1.52
		1	1	0	VOS7	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0		
		1	1	0	-	-	-	-	-	-	-	VOS8		
(CBh)	VgSorcSel	0	1	0	1	1	0	0	1	0	1	1	FV3 with Booster x2 control	9.1.53
		1	1	0	-	-	-	-	-	-	-	2BT0		
(CCh)	ID1Set	0	1	0	1	1	0	0	1	1	0	0	ID1 setting	9.1.54
		1	1	0	ID1_7	ID1_6	ID1_5	ID1_4	ID1_3	ID1_2	ID1_1	ID1_0		
(CDh)	ID2Set	0	1	0	1	1	0	0	1	1	0	1	ID2 setting	9.1.55

ST7637

		1	1	0	1	ID2_6	ID2_5	ID2_4	ID2_3	ID2_2	ID2_1	ID2_0		
(CEh)	ID3Set	0	1	0	1	1	0	0	1	1	1	0	ID3 setting	9.1.56
		1	1	0	ID3_7	ID3_6	ID3_5	ID3_4	ID3_3	ID3_2	ID3_1	ID3_0		
(D0h)	ANASET	0	1	0	1	1	0	1	0	0	0	0	Analog circuit setting	9.1.57
		1	1	0	0	0	0	1	1	1	0	1		
(D7h)	AutoLoadSet	0	1	0	1	1	0	1	0	1	1	1	mask rom data auto re-load control	9.1.58
		1	1	0	EXTE	OTPBE	-	ARD	1	1	1	1		
(DEh)	RDTstStatus	0	1	0	1	1	0	1	1	1	1	0	read IC status	9.1.59
		1	0	1	-	-	-	-	-	-	-	-	Dummy Read	
(E0h)	EPCTIN	0	1	0	1	1	1	0	0	0	0	0	Control OTP WR/RD	9.1.60
		1	1	0	0	0	WR /XRD	0	0	0	0	0		
(E1h)	EPCTOUT	0	1	0	1	1	1	0	0	0	0	1	OTP control cancel	9.1.61
(E2h)	EPMWR	0	1	0	1	1	1	0	0	0	1	0	Write to OTP	9.1.62
(E3h)	EPMRD	0	1	0	1	1	1	0	0	0	1	1	Read from OTP	9.1.63
(E4h)	OTPSEL	0	1	0	1	1	1	0	0	1	0	0	Select OTP	9.1.64
		1	1	0	MS1	MS0	0	1	1	0	0	0		
(E5h)	ROMSET	0	1	0	1	1	1	0	0	1	0	1	Programmable rom setting	9.1.65
		1	1	0	0	0	0	0	1	1	0	0		
(E7h)		0	1	0	1	1	1	0	0	1	1	1	Low voltage mode setting	9.1.66
		1	1	0	0	0	1	0	0	0	1	0		
(E8h)		0	1	0	1	1	1	0	1	0	0	0		
		1	1	0	0	0	1	1	0	1	1	1		
		1	1	0	0	0	0	0	0	0	1	1		
		1	1	0	0	0	0	1	1	1	1	1		
(EBh)	HPMSET	0	1	0	1	1	1	0	1	0	1	1	High power mode setting	9.1.67
		1	1	0	0	0	0	0	0	0	1	0		
		1	1	0	0	0	0	0	0	0	0	1		
(F0h)	FRMSEL	0	1	0	1	1	1	1	0	0	0	0	Frame Freq. in Temp range A,B,C and D	9.1.68
		1	1	0	-	-	-	FA4	FA3	FA2	FA1	FA0		
		1	1	0	-	-	-	FB4	FB3	FB2	FB1	FB0		
		1	1	0	-	-	-	FC4	FC3	FC2	FC1	FC0		
		1	1	0	-	-	-	FD4	FD3	FD2	FD1	FD0		

ST7637

(F1h)	FRM8SEL	0	1	0	1	1	1	1	0	0	0	1	Frame Freq. in Temp range A,B,C and D (idle)	9.1.69
		1	1	0	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0		
		1	1	0	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0		
		1	1	0	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0		
		1	1	0	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0		
(F2h)	TMPRNG	0	1	0	1	1	1	1	0	0	1	0	Temp range A,B and C	9.1.70
		1	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0		
		1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0		
		1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0		
(F3h)	TMPHYS	0	1	0	1	1	1	1	0	0	1	1	Hysteresis value set	9.1.71
		1	1	0	-	-	-	-	TH3	TH2	TH1	TH0		
(F4h)	TEMPSEL	0	1	0	1	1	1	1	0	1	0	0	TEMPSEL	9.1.72
		1	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00		
		1	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20		
		1	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40		
		1	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60		
		1	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80		
		1	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0		
		1	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0		
		1	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0		
(F7h)	THYS	0	1	0	1	1	1	1	0	1	1	1	Temperature detection threshold	9.1.73
		1	1	0	THYS7	THYS6	THYS5	THYS4	THYS3	THYS2	THYS1	THYS0		
(F9h)	Frame Set	0	1	0	1	1	1	1	1	0	0	1	Set Frame RGB value	9.1.74
		1	1	0	-	-	-	P14	P13	P12	P11	P10		
		1	1	0	-	-	-	P24	P23	P22	P21	P20		
		:	:	:	:	:	:	:	:	:	:	:		
		1	1	0	-	-	-	P154	P153	P152	P151	P150		
		1	1	0	-	-	-	P164	P163	P162	P161	P160		

ST7637

OTPB related register list

Register	Function
0xB7[3]	BGR setting
0xB7[6]	MX setting
0xC3[2:0]	Bias setting
0xC4[2:0]	Booster setting
0xC5[1:0]	Booster efficiency setting
0xCB[0]	Vg source control
0xCC[7:0]	ID1 setting
0xCE[7:0]	ID3 setting

OTP related register list

Register	Function
0xB5[7:0]	N-line setting
0xC7[8:0]	Vop offset setting
0xCD[6:0]	ID2 setting
0xD7[6]	OTPB auto-read enable
0xD7[7]	External command enable

ST7637

9.1.1. NOP(00h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NOP	0	1	0	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter											

Description	This command is an empty command. It does not have effect on the display module. However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands.	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	N/A
	S/W Reset	N/A
	H/W Reset	N/A
Flow Chart	-	

9.1.2. SWRESET: Software Reset (01h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SWRESET	0	1	0	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter											

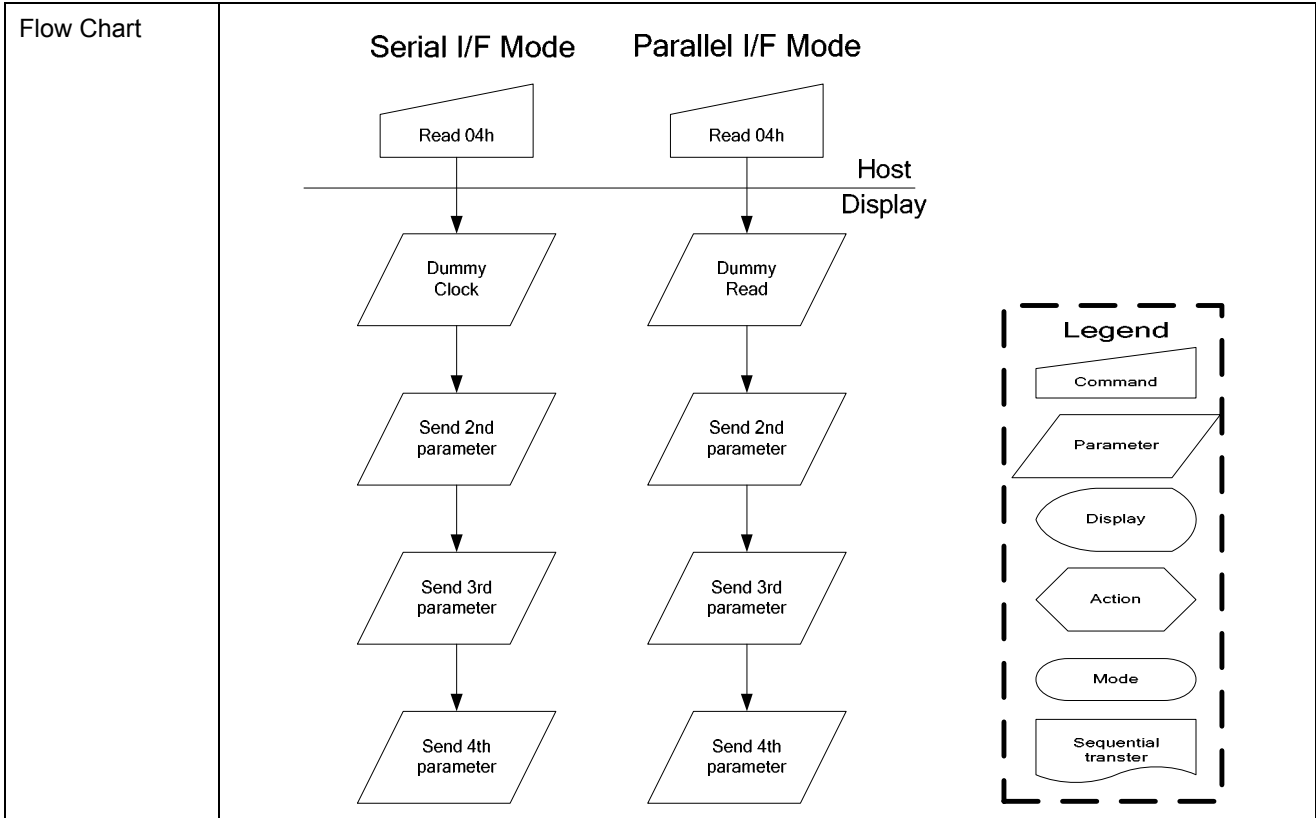
Description	<p>When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all segment & common outputs are set to Vm (display off: blank display). (See default tables in each command description)</p> <p><i>Note: The Frame Memory contents are not affected by this command.</i></p>													
Restriction	<p>It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command.</p> <p>Software Reset command cannot be sent during Sleep Out sequence.</p>													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A					
Status	Default Value													
Power On Sequence	N/A													
S/W Reset	N/A													
H/W Reset	N/A													
Flow Chart	<pre> graph TD SWRESET[SWRESET] --> Display[Display whole blank screen] Display --> Set[Set Commands to S/W Default Value] Set --> Sleep[Sleep In Mode] </pre>													

9.1.3. RDDID: Read Display ID (04h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDID	0	1	0	0	0	0	0	0	1	0	0	(04h)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2 nd parameter	1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
3 rd parameter	1	0	1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
4 th parameter	1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: “-“ Don’t care

Description	<p>This read byte returns 24-bit display identification information.</p> <p>The 1st parameter is dummy data</p> <p>The 2nd parameter (ID17 to ID10): LCD module’s manufacturer ID.</p> <p>The 3rd parameter (ID26 to ID20): LCD module/driver version ID</p> <p>The 4th parameter (ID37 to ID30): LCD module/driver ID.</p> <p>NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.</p>			
Restriction				
Register Availability	Status	Availability		
	Normal Mode On, Idle Mode Off, Sleep Out	Yes		
	Normal Mode On, Idle Mode On, Sleep Out	Yes		
	Partial Mode On, Idle Mode Off, Sleep Out	Yes		
	Partial Mode On, Idle Mode On, Sleep Out	Yes		
	Sleep In	Yes		
Default	Status	Default Value		
		ID1	ID2	ID3
	Power On Sequence	TBD	TBD	TBD
	S/W Reset	TBD	TBD	TBD
	H/W Reset	TBD	TBD	TBD



9.1.4. RDDST: Read Display Status (09h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDST	0	1	0	0	0	0	0	1	0	0	1	(09h)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2 nd parameter	1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-
3 rd parameter	1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-
4 th parameter	1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-
5 th parameter	1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-

NOTE: "- " Don't care

Description	This command indicates the current status of the display as described in the table below:		
	Bit	Description	Value
	ST31	Booster Voltage Status	"1"=Booster on, "0"=off
	ST30	Row Address Order (MY)	"1"=Decrement, "0"=Increment
	ST29	Column Address Order (MX)	"1"=Decrement, "0"=Increment
	ST28	Row/Column Order (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
	ST27	Scan Address Order (ML)	"1"=Decrement, "0"=Increment
	ST26	RGB/BGR Order (RGB)	"1"=BGR, "0"=RGB
	ST25	Not Used	"0"
	ST24	Not Used	"0"
	ST23	Not Used	"0"
	ST22	Interface Color Pixel Format Definition	"010" = 8-bit / pixel, "011" = 12-bit / pixel type A "100" = 12-bit / pixel type B "101" = 16-bit / pixel, "110" = 18-bit / pixel, "111" = 24-bit / pixel
	ST21		
	ST20		
	ST19	Idle Mode On/Off	"1" = On, "0" = Off
	ST18	Partial Mode On/Off	"1" = On, "0" = Off
	ST17	Sleep In/Out	"1" = Out, "0" = In
	ST16	Display Normal Mode On/Off	"1" = Normal Display, "0" = Partial Display
	ST15	Vertical Scrolling Status	"1" = Scroll on, "0" = Scroll off
	ST14	Not Used	"0"
	ST13	Inversion Status	"1" = On, "0" = Off
	ST12	All Pixels On	"1" = all pixel on, "0" = normal display
	ST11	All Pixels Off	"1" = all pixel off, "0" = normal display
	ST10	Display On/Off	"1" = On, "0" = Off
	ST9	Tearing effect line on/off	"1" = On, "0" = Off
	ST8	Not Used	"0"
	ST7	Not Used	"0"
	ST6	Not Used	"0"
	ST5	Tearing effect line mode	"0" = mode1, "1" = mode2
	ST4	Not Used	"0"
	ST3	Not Used	"0"
	ST2	Not Used	"0"

	ST0	Not Used	"0"
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value (ST[31:0])	
	Power On Sequence	0000 0000_0101 0001_0000 0000_0000 0000	
	S/W Reset	0xxx xx00_0xxx 0001_0000 0000_0000 0000	
	H/W Reset	0000 0000_0101 0001_0000 0000_0000 0000	
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p> </div> </div> <div style="margin-top: 20px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>		

9.1.5. RDDPM: Read Display Power Mode (0Ah)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDPM	0	1	0	0	0	0	0	1	0	1	0	(0Ah)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	D6	D5	D4	D3	D2	0	0	-

NOTE: “-“ Don’t care

Description	This command indicates the current status of the display as described in the table below:	
	Bit	Description
	D7	Booster Voltage Status
	D6	Idle Mode On/Off
	D5	Partial Mode On/Off
	D4	Sleep In/Out
	D3	Display Normal Mode On/Off
	D2	Display On/Off
	D1	Not Used
D0	Not Used	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (D[7:0])
	Power On Sequence	00001000b (08h)
	S/W Reset	00001000b (08h)
	H/W Reset	00001000b (08h)
Flow Chart	Serial I/F Mode	Parallel I/F Mode

9.1.6. RDDMADCTR: Read Display MADCTR (0Bh)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDMADCTR	0	1	0	0	0	0	0	1	0	1	1	(0Bh)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	D6	D5	D4	D3	0	0	0	-

NOTE: “-“ Don't care

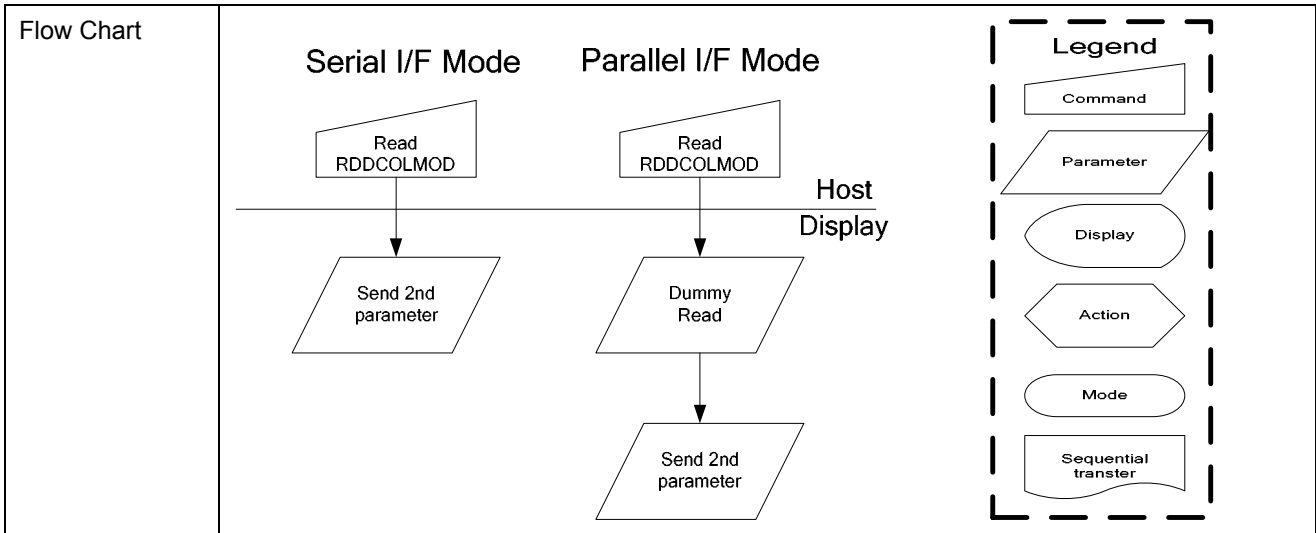
Description	This command indicates the current status of the display as described in the table below:	
	Bit	Description
	D7	Row Address Order (MY)
	D6	Column Address Order (MX)
	D5	Row/Column Order (MV)
	D4	Scan Address Order (ML)
	D3	RGB/BGR Order (RGB)
	D2	Not Used
	D1	Not Used
D0	Not Used	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (D[7:0])
	Power On Sequence	00h
	S/W Reset	No change
	H/W Reset	00h
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> <pre> graph TD A[/Read RDDMADCTL/] --> B[/Send 2nd parameter/] </pre> </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p> <pre> graph TD A[/Read RDDMADCTL/] --> B[/Dummy Read/] B --> C[/Send 2nd parameter/] </pre> </div> </div>	
	<div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>	

9.1.7. RDDCOLMOD: Read Display Pixel Format (0Ch)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDCOLMOD	0	1	0	0	0	0	0	1	1	0	0	(0Ch)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2 nd parameter	1	0	1	0	0	0	0	0	D2	D1	D0	-

NOTE: “-“ Don’t care

Description	This command indicates the current status of the display as described in the table below:	
	Bit	Description
	D7	RGB Interface Color Format
	D6	
	D5	
	D4	
	D3	Control Interface Color Format
	D2	
D1		
D0		
		Value
		“0” (Not Used)
		“0” (Not Used)
		“0” (Not Used)
		“0” (Not Used)
		“0”
		“010”=8 bit/pixel “011”=12 bit/pixel (type A) “100”=12 bit/pixel (type B) “101”=16 bit/pixel “110” = 18-bit/pixel “111” = 24-bit/pixel The others = not defined
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (D[7:0])
	Power On Sequence	16 bit/pixel
	S/W Reset	No change
	H/W Reset	16 bit/pixel

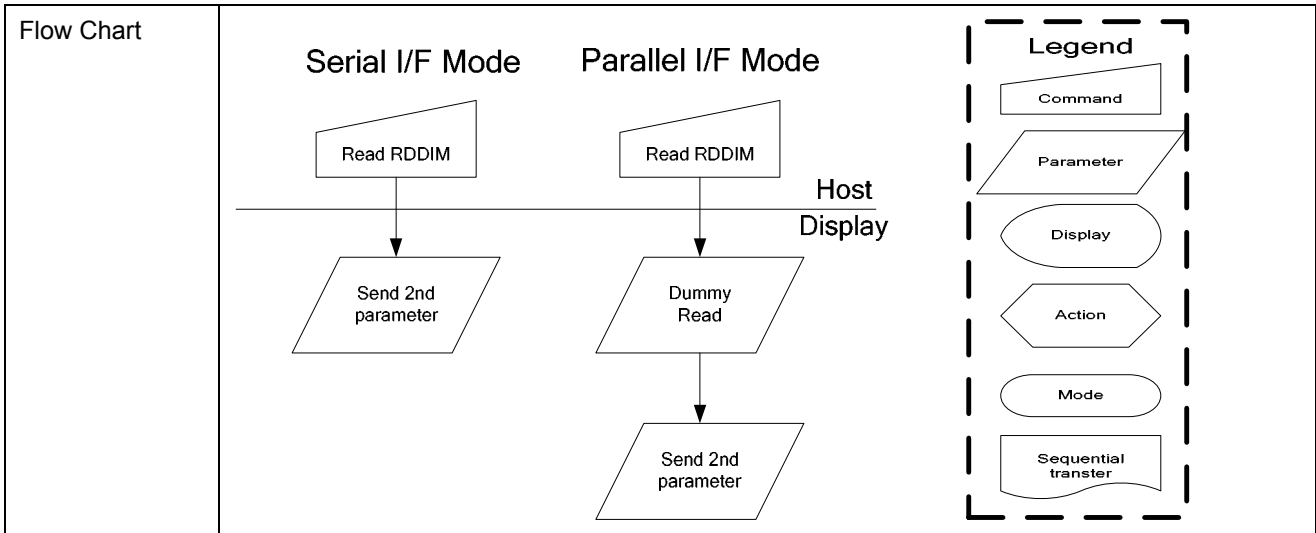


9.1.8. RDDIM: Read Display Image Mode (0Dh)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDIM	0	1	0	0	0	0	0	1	1	0	1	(0Dh)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2 nd parameter	1	0	1	D7	0	D5	D4	D3	0	0	0	-

NOTE: “-“ Don’t care

Description	This command indicates the current status of the display as described in the table below:	
	Bit	Description
	D7	Vertical Scrolling On/Off
	D6	Not Used
	D5	Inversion On/Off
	D4	All Pixels On
	D3	All Pixels Off
	D2	Not Used
D1		
D0		
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (D[7:0])
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h



9.1.9. RDDSM: Read Display Signal Mode (0Eh)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDSM	0	1	0	0	0	0	0	1	1	1	0	(0Eh)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	D7	D6	0	0	0	0	0	0	-

NOTE: “-“ Don't care

Description	This command indicates the current status of the display as described in the table below:	
	Bit	Description
	D7	Tearing Effect Line On/Off
	D6	Tearing effect line mode
	D5	Not Used
	D4	Not Used
	D3	Not Used
	D2	Not Used
	D1	Not Used
D0	Not Used	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (D[7:0])
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	Serial I/F Mode	Parallel I/F Mode

9.1.10. RDDSDR: Read Display Self-Diagnostic Result (0Fh)

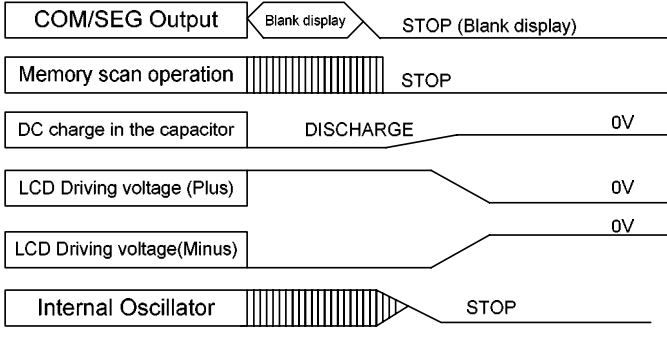
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDSDR	0	1	0	0	0	0	0	1	1	1	1	(0Fh)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2 nd parameter	1	0	1	D7	D6	0	D4	0	0	0	0	

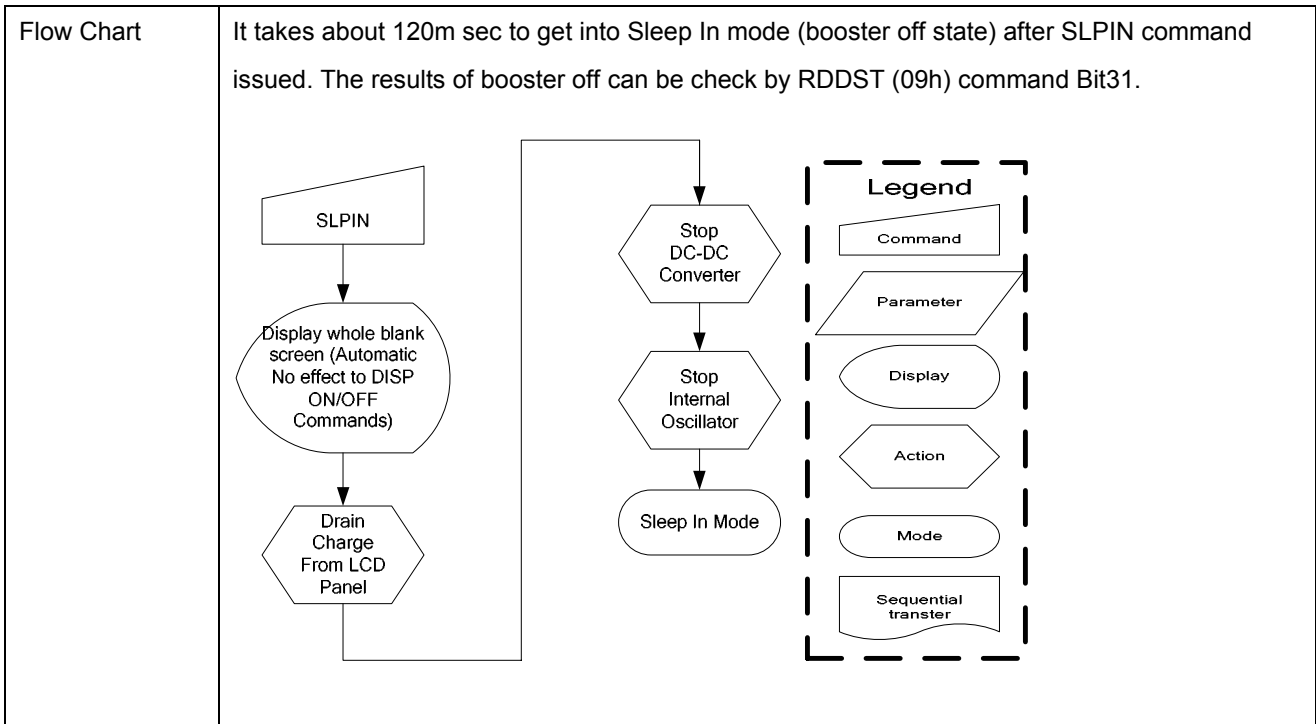
NOTE: “-“ Don't care

Description	This command indicates the current status of the display as described in the table below:	
	Bit	Description
	D7	Register Loading Detection
	D6	Functionality Detection
	D5	Not Used
	D4	Glass broken Detection
	D3	Not Used
	D2	Not Used
	D1	Not Used
D0	Not Used	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (D[7:0])
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	Serial I/F Mode	Parallel I/F Mode

9.1.11. SLPIN: Sleep In (10h)

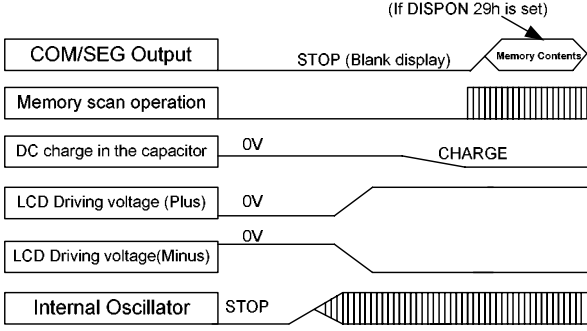
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SLPIN	0	1	0	0	0	0	1	0	0	0	0	(10h)
Parameter	No Parameter											

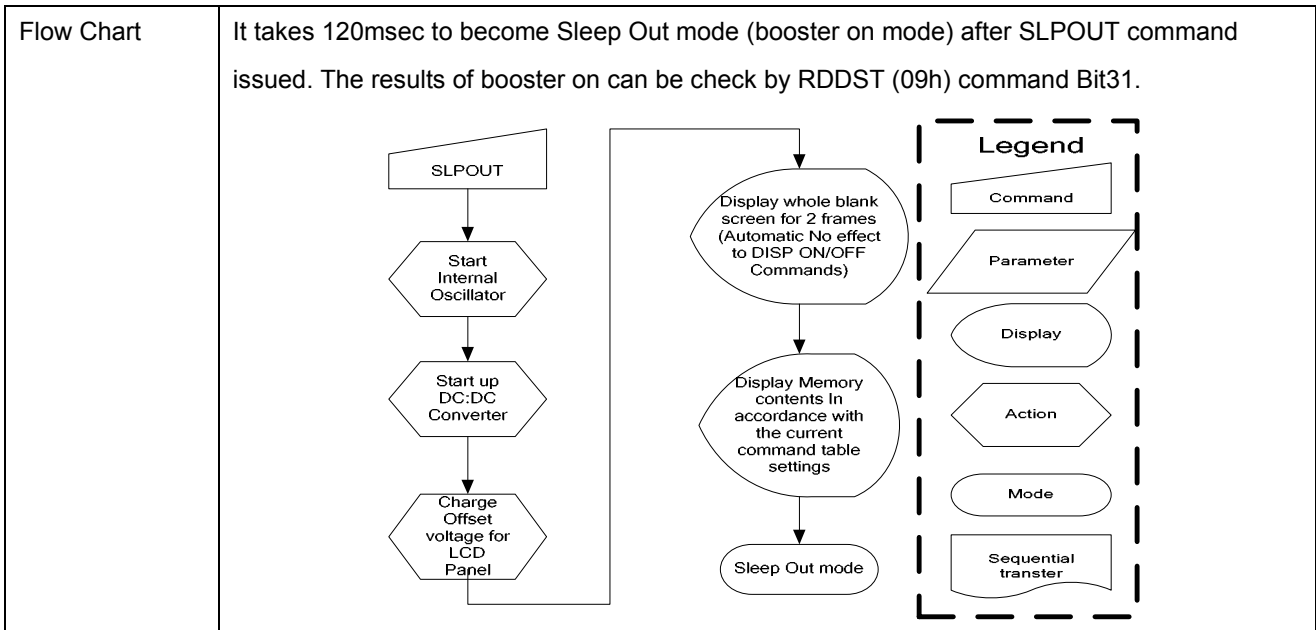
Description	<p>This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.</p>  <p>MCU interface and memory are still working and the memory keeps its contents</p>													
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).</p> <p>It will be necessary to wait 5msec before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize.</p> <p>It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep in mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep in mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep in mode</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Sleep in mode	S/W Reset	Sleep in mode	H/W Reset	Sleep in mode					
Status	Default Value													
Power On Sequence	Sleep in mode													
S/W Reset	Sleep in mode													
H/W Reset	Sleep in mode													



9.1.12. SLPOUT: Sleep Out (11h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SLPOUT	0	1	0	0	0	0	1	0	0	0	1	(11h)
Parameter	No Parameter											

Description	<p>This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.</p> 													
Restriction	<p>This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).</p> <p>It will be necessary to wait 5msec before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize.</p> <p>The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.</p> <p>The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p>													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep in mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep in mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep in mode</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Sleep in mode	S/W Reset	Sleep in mode	H/W Reset	Sleep in mode					
Status	Default Value													
Power On Sequence	Sleep in mode													
S/W Reset	Sleep in mode													
H/W Reset	Sleep in mode													



ST7637

9.1.13. PTLON: Partial Display Mode On (12h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PTLON	0	1	0	0	0	0	1	0	0	1	0	(12h)
Parameter	No Parameter											

Description	<p>This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h)</p> <p>Exit from PTLON by Normal Display Mode On command (13H)</p> <p>There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.</p>													
Restriction	This command has no effect when Partial mode is active.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Partial mode off</td> </tr> <tr> <td>S/W Reset</td> <td>Partial mode off</td> </tr> <tr> <td>H/W Reset</td> <td>Partial mode off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Partial mode off	S/W Reset	Partial mode off	H/W Reset	Partial mode off					
Status	Default Value													
Power On Sequence	Partial mode off													
S/W Reset	Partial mode off													
H/W Reset	Partial mode off													
Flow Chart	See Partial Area (30h)													

ST7637

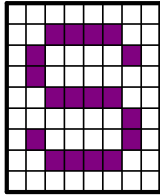
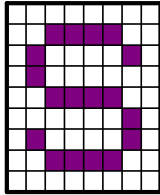
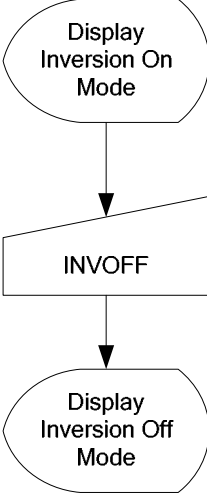






9.1.14. NORON: Normal Display Mode On (13h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NORON	0	1	0	0	0	0	1	0	0	1	1	(13h)
Parameter	No Parameter											

Description	<p>This command returns the display to normal mode.</p> <p>Normal display mode on means Partial mode off, Scroll mode Off.</p> <p>Exit from NORON by the Partial mode On command (12h)</p> <p>There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.</p>	
Restriction	This command has no effect when Normal Display mode is active.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	Normal Mode On
	S/W Reset	Normal Mode On
	H/W Reset	Normal Mode On
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command	

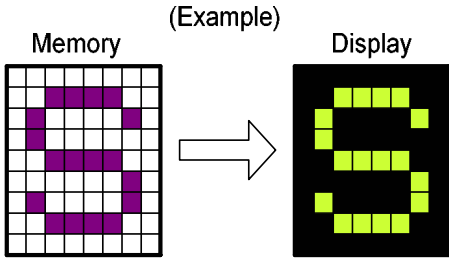
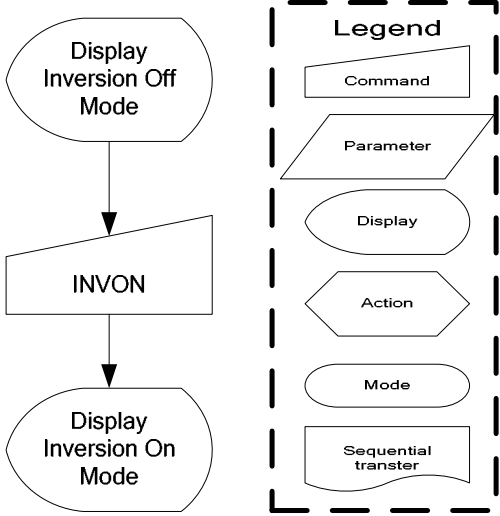
9.1.15. INVOFF: Display Inversion Off (20h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVOFF	0	1	0	0	0	1	0	0	0	0	0	(20h)
Parameter	No Parameter											

Description	<p>This command is used to recover from display inversion mode.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p>	
	<p style="text-align: center;">(Example)</p> <div style="display: flex; justify-content: center; align-items: center;"> <div style="text-align: center;"> <p>Memory</p>  </div> <div style="margin: 0 20px;"> <p>→</p> </div> <div style="text-align: center;"> <p>Display</p>  </div> </div>	
Restriction	This command has no effect when module is already inversion off mode.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	Display Inversion off
	S/W Reset	Display Inversion off
	H/W Reset	Display Inversion off
Flow Chart	<div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;">  </div> <div style="margin-left: 20px;"> <p>Legend</p> <ul style="list-style-type: none">  Command  Parameter  Display  Action  Mode  Sequential transfer </div> </div>	

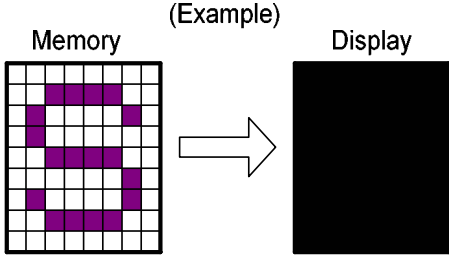
9.1.16. INVON: Display Inversion On (21h)

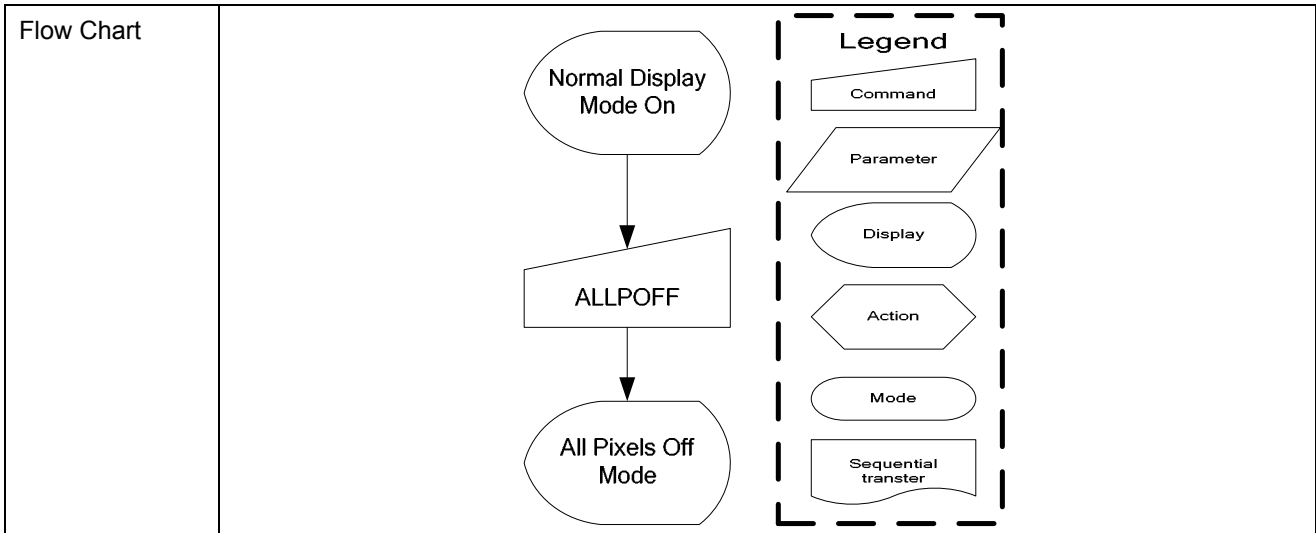
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVON	0	1	0	0	0	1	0	0	0	0	1	(21h)
Parameter	No Parameter											

Description	<p>This command is used to enter into display inversion mode</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p>To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.</p>													
	<p>(Example)</p> 													
Restriction	This command has no effect when module is already Inversion On mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Inversion off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Inversion off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off					
Status	Default Value													
Power On Sequence	Display Inversion off													
S/W Reset	Display Inversion off													
H/W Reset	Display Inversion off													
Flow Chart														

9.1.17. APOFF: All Pixels Off (22h) (Only for Test Purposes)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
APOFF	0	1	0	0	0	1	0	0	0	1	0	(22h)
Parameter	No Parameter											

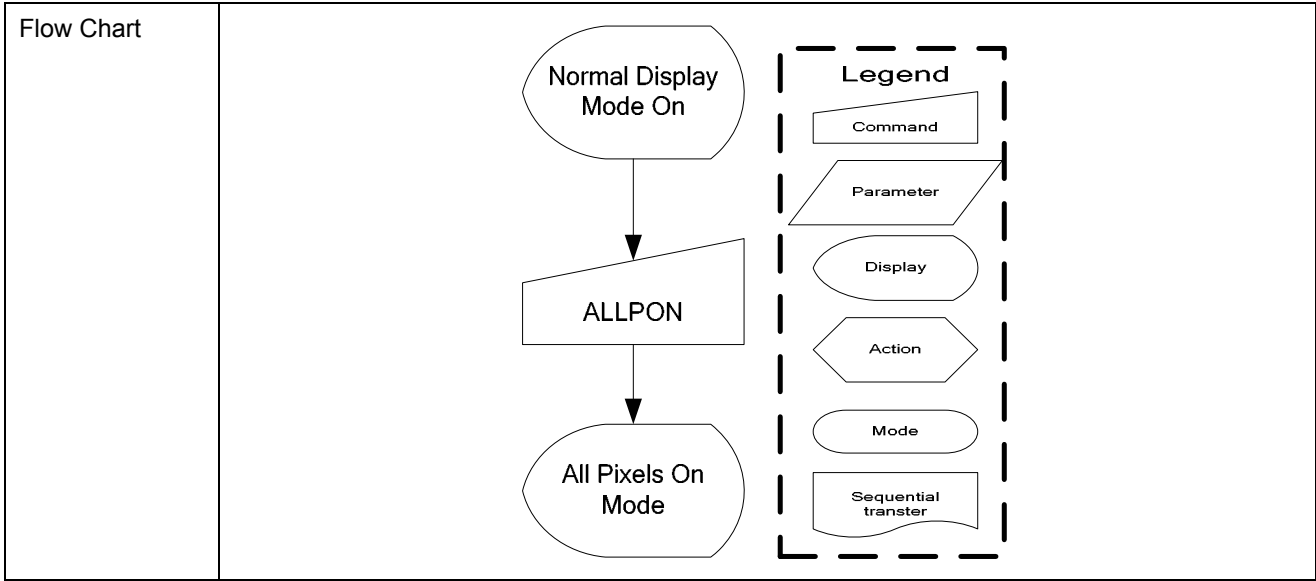
Description	<p>This command is only used for test purpose e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software.</p> <p>All driver outputs become “Low” data state and display becomes black.</p> <p>This command makes no change of contents of display memory.</p> <p>This command does not change any other status.</p> <p>Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”.</p> <p>The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands.</p> <div style="text-align: center;">  <p>(Example)</p> </div>													
Restriction	This command has no effect when module is already All Pixel Off mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>All pixel off mode disable</td> </tr> <tr> <td>S/W Reset</td> <td>All pixel off mode disable</td> </tr> <tr> <td>H/W Reset</td> <td>All pixel off mode disable</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	All pixel off mode disable	S/W Reset	All pixel off mode disable	H/W Reset	All pixel off mode disable					
Status	Default Value													
Power On Sequence	All pixel off mode disable													
S/W Reset	All pixel off mode disable													
H/W Reset	All pixel off mode disable													



9.1.18. APON: All Pixels On (23h) (Only for Test Purposes)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
APON	0	1	0	0	0	1	0	0	0	1	1	(23h)
Parameter	No Parameter											

Description	<p>This command is only used for test purpose e.g. pixel response time (on/off) measurements on the passive matrix display. Therefore, it is possible that this command is not used for final product software.</p> <p>All driver outputs become “High” data state and display becomes white.</p> <p>This command makes no change of contents of display memory.</p> <p>This command does not change any other status.</p> <p>Exit commands are “All Pixels On”, “Normal Display Mode On” and “Partial Display On”.</p> <p>The display is showing the contents of the frame memory after “Normal Display Mode On” and “Partial Display On” commands.</p>													
Restriction	This command has no effect when module is already All Pixel On mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>All pixel on mode disable</td> </tr> <tr> <td>S/W Reset</td> <td>All pixel on mode disable</td> </tr> <tr> <td>H/W Reset</td> <td>All pixel on mode disable</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	All pixel on mode disable	S/W Reset	All pixel on mode disable	H/W Reset	All pixel on mode disable					
Status	Default Value													
Power On Sequence	All pixel on mode disable													
S/W Reset	All pixel on mode disable													
H/W Reset	All pixel on mode disable													



9.1.19. WRCNTR: Write Contrast (25h)

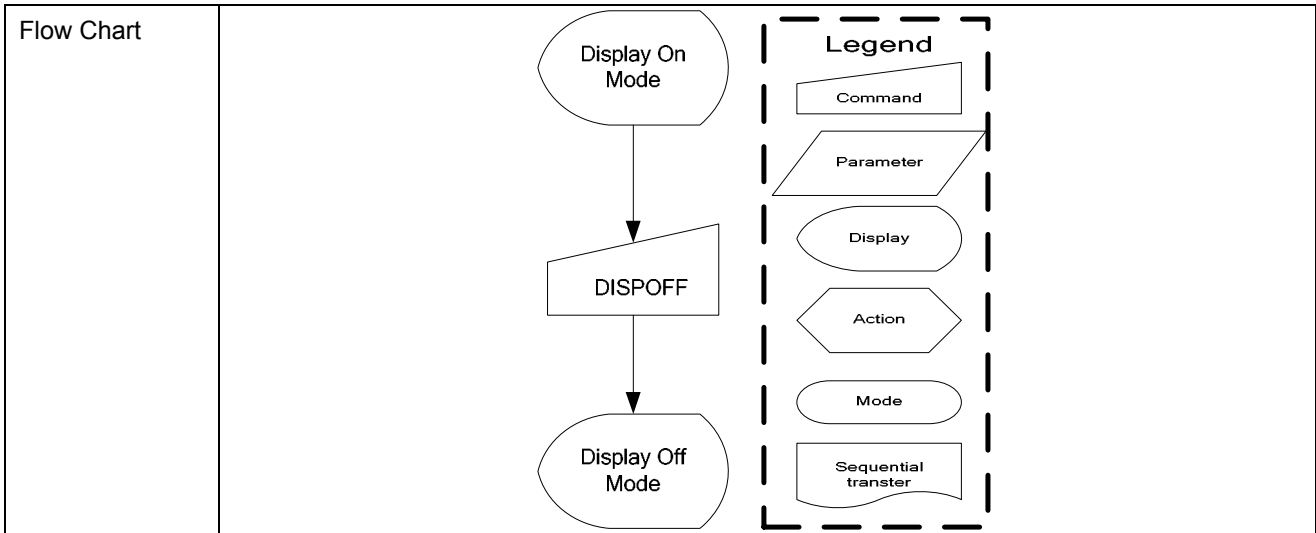
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRCNTR	0	1	0	0	0	1	0	0	1	0	1	(25h)
Parameter	1	1	0	0	EV6	EV5	EV4	EV3	EV2	EV1	EV0	

Description	This command is used to fine tuning the contrast of the display. Parameter range is 00~7Fh. The contrast is not linear but the contrast adjustment is linear. Luminance is increasing from 00h to 7Fh. 00h is presenting dark end and 7Fh is presenting bright end.	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	3Fh
	S/W Reset	3Fh
	H/W Reset	3Fh
Flow Chart	<pre> graph TD WRCNTR[Command] --> EV[Parameter EV[7:0]] EV --> NewContrast[Action: New Contrast Value Loaded] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle with slanted top Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Horizontal oval Sequential transfer: Wavy rectangle 	

9.1.20. DISPOFF: Display Off (28h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISPOFF	0	1	0	0	0	1	0	1	0	0	0	(28h)
Parameter	No Parameter											

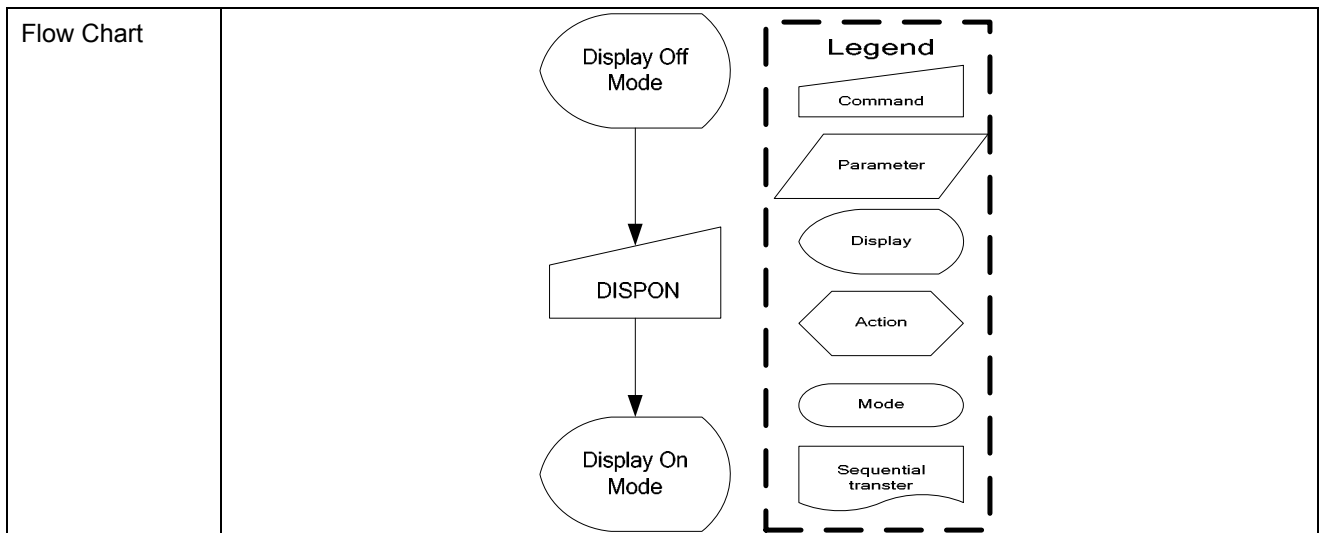
Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory disables and blank page inserted.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p>There will be no abnormal visible effect on the display.</p> <p>Exit from this command by Display On (29h)</p>													
	<p>(Example)</p>													
Restriction	This command has no effect when module is already in Display Off mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off					
Status	Default Value													
Power On Sequence	Display off													
S/W Reset	Display off													
H/W Reset	Display off													



9.1.21. DISPON: Display On (29h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISPON	0	1	0	0	0	1	0	1	0	0	1	(29h)
Parameter	No Parameter											

Description	Turn on the display screen according to the current display data RAM content and the display timing and setting.	
	<p>This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p>	
	<p>(Example)</p>	
Restriction	This command has no effect when module is already in Display On mode.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	Display off
	S/W Reset	Display off
	H/W Reset	Display off

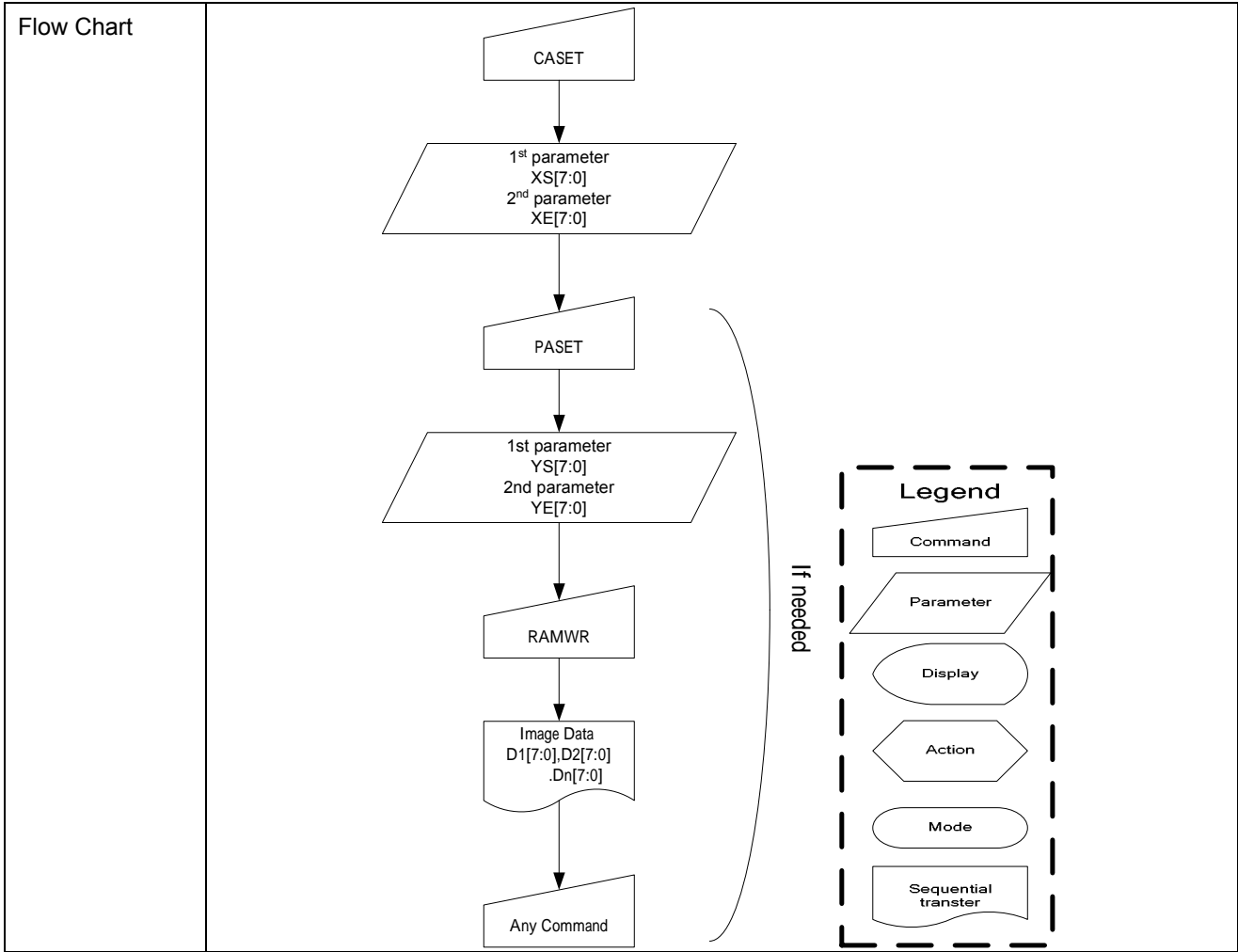


9.1.22. CASET: Column Address Set (2Ah)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CASET	0	1	0	0	0	1	0	1	0	1	0	(2Ah)
1st Parameter	1	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
2nd Parameter	1	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

NOTE: “-“ Don't care

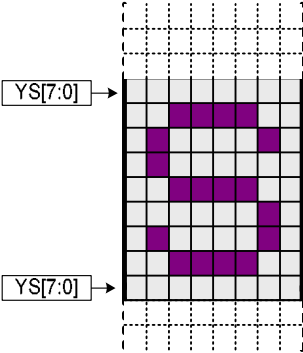
Description	<p>This command is used to define area of frame memory where MCU can access.</p> <p>This command makes no change on the other driver status.</p> <p>The value of XS [7:0] and XE [7:0] are referred when RAMWR command comes.</p> <p>Each value represents one column line in the Frame Memory.</p> <p style="text-align: center;">(Example)</p> <div style="text-align: center;"> </div>															
Restriction	<p>XS [7:0] always must be equal to or less than XE [7:0]</p> <p>When XS [7:0] or XE [7:0] is greater than 83h, data of out of range will be ignored.</p>															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
Normal Mode On, Idle Mode On, Sleep Out	Yes															
Partial Mode On, Idle Mode Off, Sleep Out	Yes															
Partial Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>XS [7:0]</th> <th>XE [7:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> <td>83h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> <td>83h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> <td>83h</td> </tr> </tbody> </table>	Status	Default Value		XS [7:0]	XE [7:0]	Power On Sequence	00h	83h	S/W Reset	00h	83h	H/W Reset	00h	83h	
Status	Default Value															
	XS [7:0]	XE [7:0]														
Power On Sequence	00h	83h														
S/W Reset	00h	83h														
H/W Reset	00h	83h														



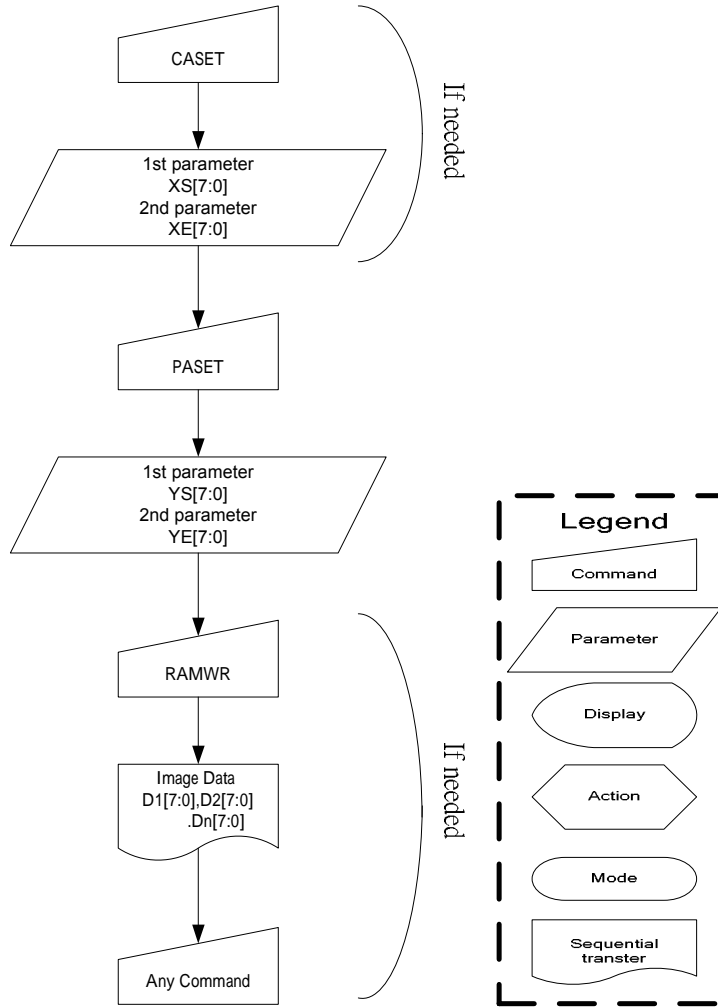
9.1.23. RASET: Row Address Set (2Bh)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RASET	0	1	0	0	0	1	0	1	0	1	1	(2Bh)
1st Parameter	1	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
2nd Parameter	1	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

NOTE: “-“ Don't care

Description	<p>This command is used to define area of frame memory where MCU can access.</p> <p>This command makes no change on the other driver status.</p> <p>The value of YS [7:0] and YE [7:0] are referred when RAMWR command comes.</p> <p>Each value represents one column line in the Frame Memory.</p> <p style="text-align: center;">(Example)</p> 															
Restriction	<p>YS [7:0] always must be equal to or less than YE [7:0]</p> <p>When YS [7:0] or YE [7:0] is greater than 83h, data of out of range will be ignored.</p>															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
Normal Mode On, Idle Mode On, Sleep Out	Yes															
Partial Mode On, Idle Mode Off, Sleep Out	Yes															
Partial Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>XS [7:0]</th> <th>XE [7:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> <td>83h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> <td>83h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> <td>83h</td> </tr> </tbody> </table>	Status	Default Value		XS [7:0]	XE [7:0]	Power On Sequence	00h	83h	S/W Reset	00h	83h	H/W Reset	00h	83h	
Status	Default Value															
	XS [7:0]	XE [7:0]														
Power On Sequence	00h	83h														
S/W Reset	00h	83h														
H/W Reset	00h	83h														

Flow Chart



9.1.24. RAMWR: Memory Write (2Ch)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RAMWR	0	1	0	0	0	1	0	1	1	0	0	(2Ch)
Write D1[7:0]	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	-
:	1	1	0	:	:	:	:	:	:	:	:	-
Write Dn[7:0]	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	-

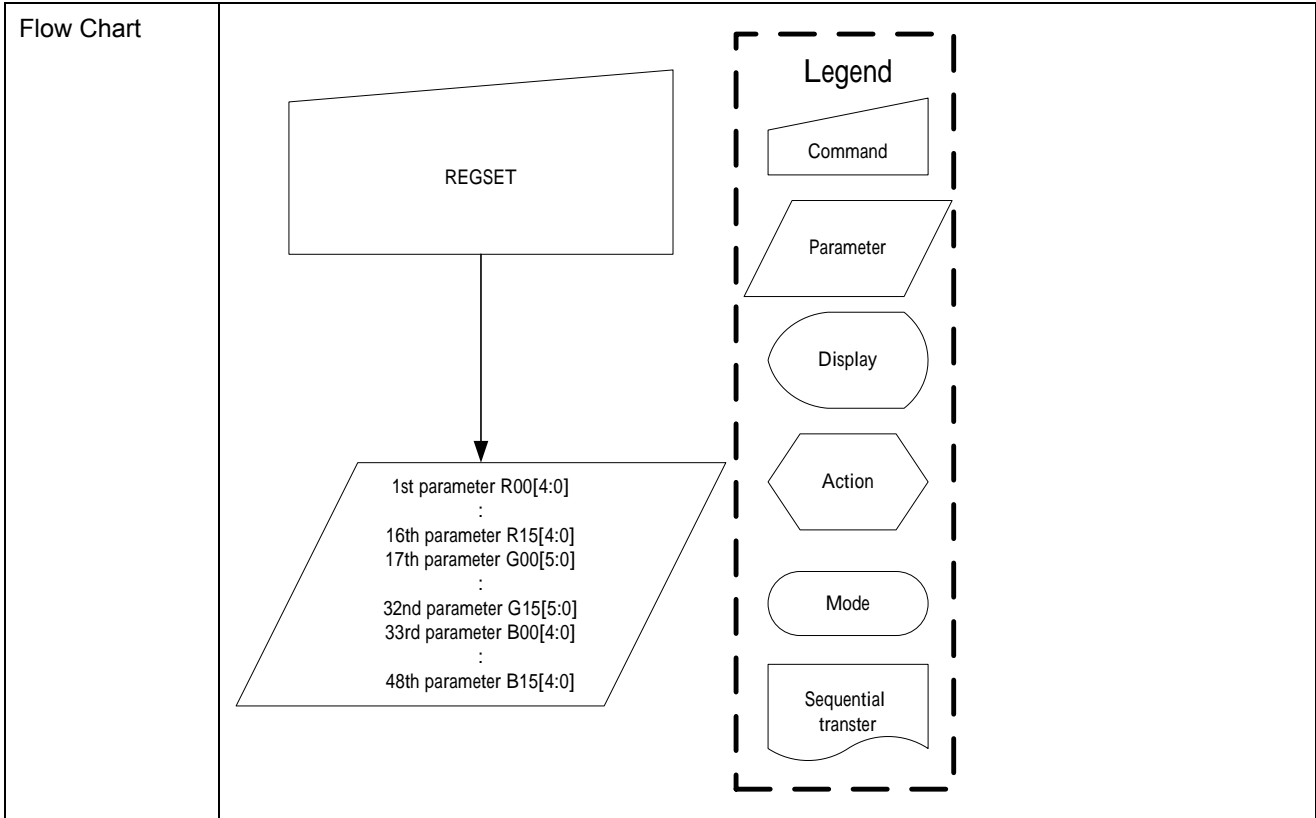
Description	<p>This command is used to transfer data MCU to frame memory.</p> <p>This command makes no change to the other driver status.</p> <p>When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.</p> <p>The Start Column/Start Row positions are different in accordance with MADCTR setting. Then D [7:0] is stored in frame memory and the column register and the row register incremented.</p> <p>Frame Write can be canceled by sending any other command.</p>													
Restriction	In all color modes, there is no restriction on length of parameters.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is remained</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is remained</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is remained	H/W Reset	Contents of memory is remained					
Status	Default Value													
Power On Sequence	Contents of memory is set randomly													
S/W Reset	Contents of memory is remained													
H/W Reset	Contents of memory is remained													
Flow Chart	<pre> graph TD RAMWR[RAMWR] --> ImageData[/Image Data D1[7:0], D2[7:0]Dn[7:0]/] ImageData --> AnyCommand[Any Command] </pre>													

9.1.25. RGBSET: Colour Set for 256 or 4k-Color Display (2Dh)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RGBSET	0	1	0	0	0	1	0	1	1	0	1	(2Dh)
1 st parameter	1	1	0	-	-	-	R004	R003	R002	R001	R000	-
:	1	1	0	:	:	:	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	-
16 th parameter	1	1	0	-	-	-	R154	R153	R152	R151	R150	-
17 th parameter	1	1	0	-	-	G005	G004	G003	G002	G001	G000	-
:	1	1	0	:	:	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	-
32 nd parameter	1	1	0	-	-	G155	G154	G153	G152	G151	G150	-
33 rd parameter	1	1	0	-	-	-	B004	B003	B002	B001	B000	-
:	1	1	0	:	:	:	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	-
48 th parameter	1	1	0	-	-	-	B154	B153	B152	B151	B150	-

NOTE: “-“ Don't care

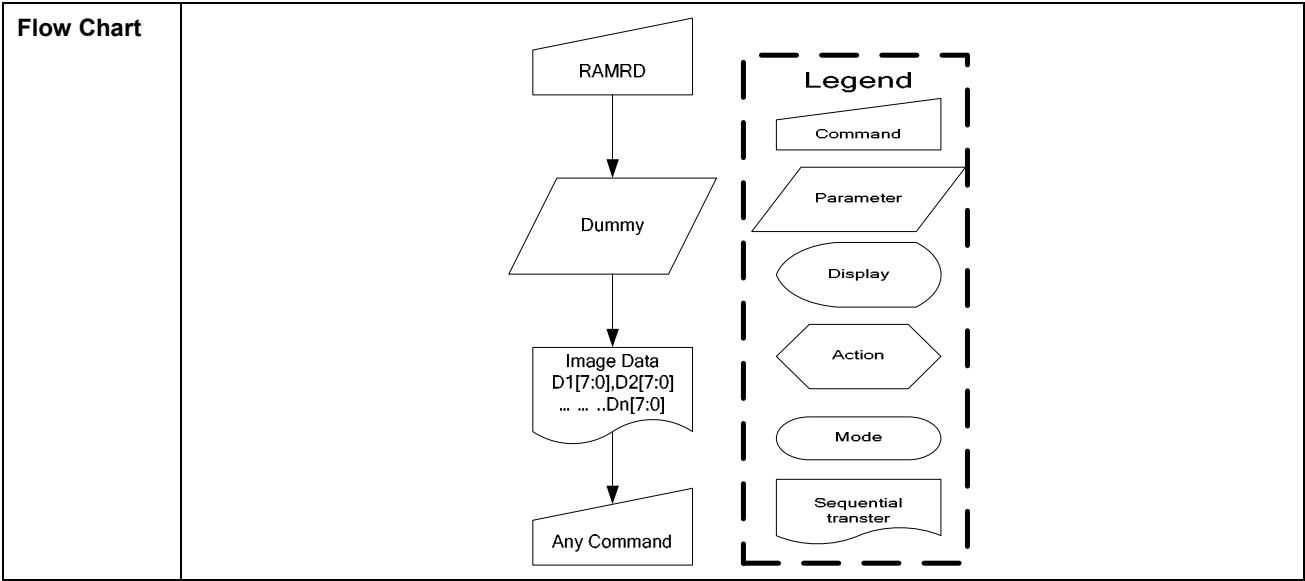
Description	<p>This command is used to define the LUT for 8bit-to-16bit or 12bit-to-16bit color depth conversations. (See also Section 7.9.)</p> <p>48 Bytes must be written to the LUT regardless of the color mode. Only the values in Section 7.9. are referred.</p> <p>This command has no effect on other commands/parameters and Contents of frame memory. Visible change takes effect next time the Frame Memory is written to.</p>													
Restriction	Do not send any command before the last data is sent or LUT is not defined correctly.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Refer to Section 7.9.</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of the look-up table protected</td> </tr> <tr> <td>H/W Reset</td> <td>Refer to Section 7.9.</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Refer to Section 7.9.	S/W Reset	Contents of the look-up table protected	H/W Reset	Refer to Section 7.9.					
Status	Default Value													
Power On Sequence	Refer to Section 7.9.													
S/W Reset	Contents of the look-up table protected													
H/W Reset	Refer to Section 7.9.													



9.1.26. RAMRO : Memory Read (2EH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	1	1	0	(2Eh)
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x
2nd parameter	1	↑	1	D17	D16	D15	D14	D13	D12	D11	D10	00H ~ FFH
...	1	↑	1	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00H ~ FFH
(N+1)th parameter	1	↑	1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00H ~ FFH

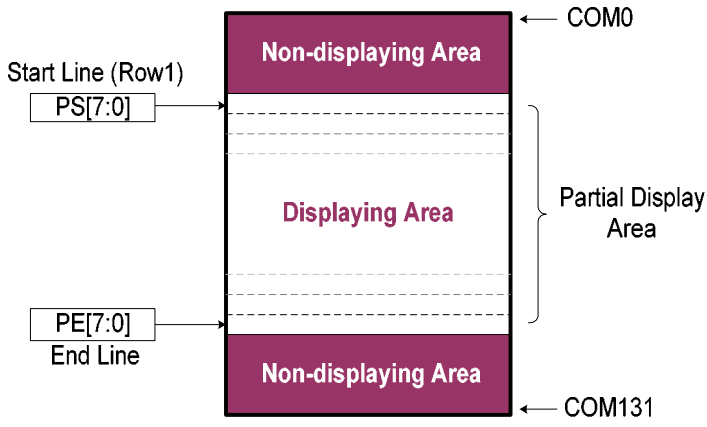
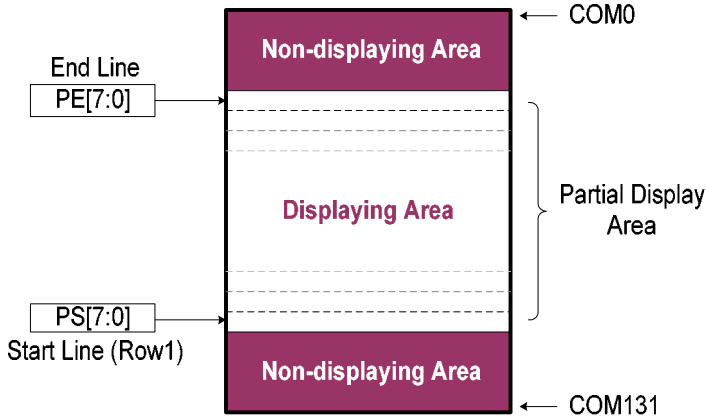
Description	This command is used to transfer data from frame memory to MCU. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTR setting. Then D[7:0] is read back from the frame memory and the column register and the page register incremented. Frame Read can be stopped by sending any other command.												
Restriction	In all color modes, the Frame Read is always 16bit so there is no restriction on length of parameters. <i>Note: Memory Read is only possible via the Parallel Interface.</i>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In or Booster Off	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
S/W Reset	Contents of memory is not cleared												
H/W Reset	Contents of memory is not cleared												

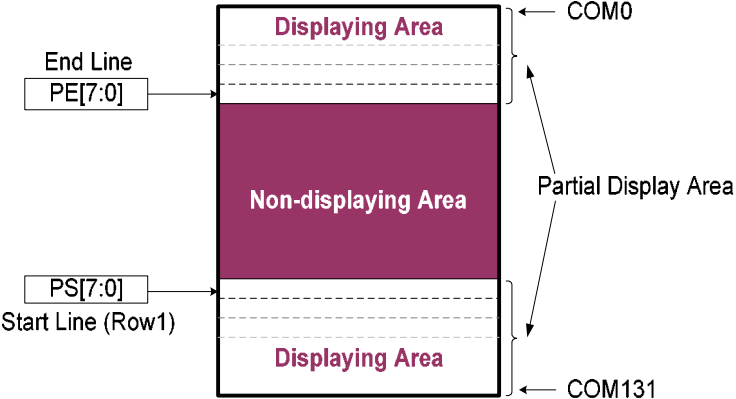


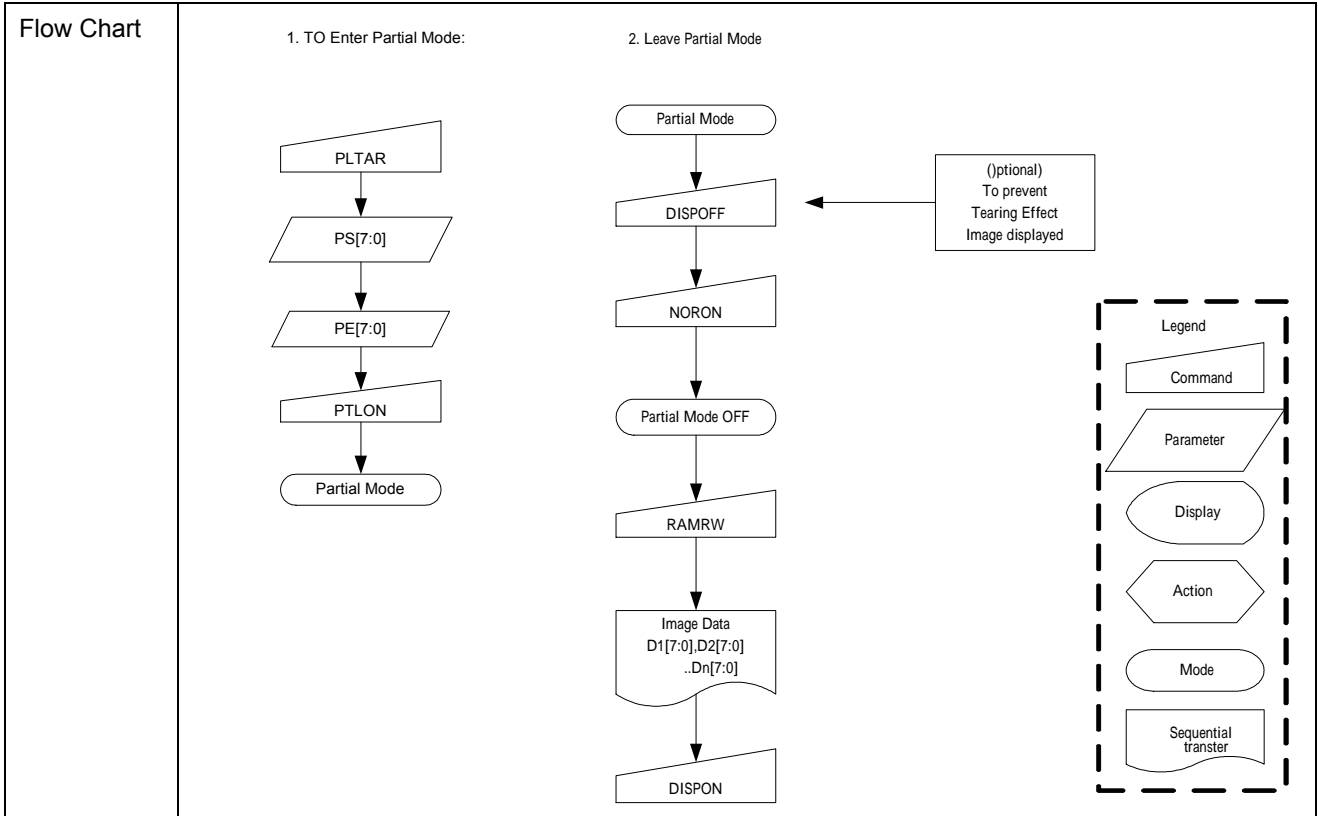
9.1.27. PTLAR: Partial Area (30h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PTLAR	0	1	0	0	0	1	1	0	0	0	0	(30h)
1st Parameter	1	1	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	-
2nd Parameter	1	1	0	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	-

NOTE: “-“ Don't care

Description	<p>This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Line (PS) and the second the End Line (PE), as illustrated in the figures below. PS and PE refer to the Frame Memory Line counter.</p> <p>If End Line > Start Line when MADCTR ML=0:</p>  <p>If End Line > Start Line when MADCTR ML=1:</p>  <p>If End Line < Start Line when MADCTR ML=0:</p>
-------------	--

	 <p>* Row1: Frame memory row address 1. If End Line = Start Line then the Partial Area will be one line deep.</p>																
Restriction	<p>PS[7:0] and PE[7:0] are based on line unit. PS[6:0]=00h, 01h, 02h, 03h, ... , 83h PE[6:0]= 00h, 01h, 02h, 03h, ... , 83h</p>																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes				
Status	Availability																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																
Normal Mode On, Idle Mode On, Sleep Out	Yes																
Partial Mode On, Idle Mode Off, Sleep Out	Yes																
Partial Mode On, Idle Mode On, Sleep Out	Yes																
Sleep In	Yes																
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>PS[6:0]</th> <th>PE[6:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> <td>83h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> <td>83h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> <td>83h</td> </tr> </tbody> </table>	Status	Default Value		PS[6:0]	PE[6:0]	Power On Sequence	00h	83h	S/W Reset	00h	83h	H/W Reset	00h	83h		
Status	Default Value																
	PS[6:0]	PE[6:0]															
Power On Sequence	00h	83h															
S/W Reset	00h	83h															
H/W Reset	00h	83h															



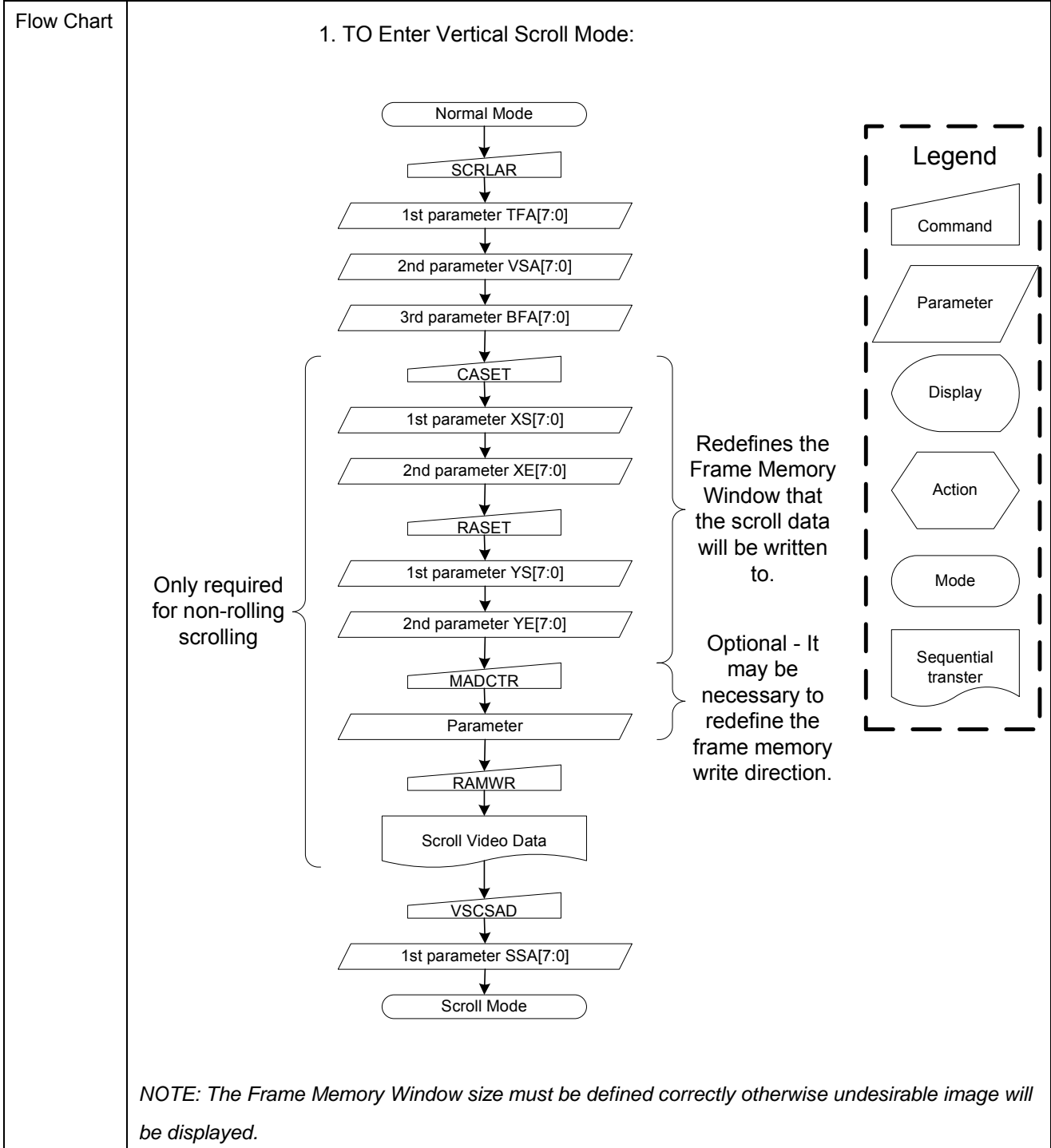
9.1.28. SCRLAR: Scroll Area (33h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SCRLAR	0	1	0	0	0	1	1	0	0	1	1	(33h)
1 st parameter	1	1	0	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-
2 nd parameter	1	1	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-
3 rd parameter	1	1	0	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-

NOTE: “-“ Don’t care

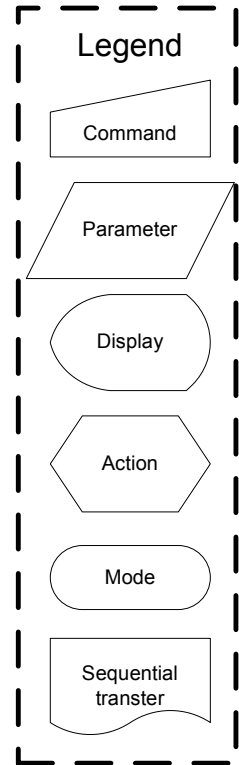
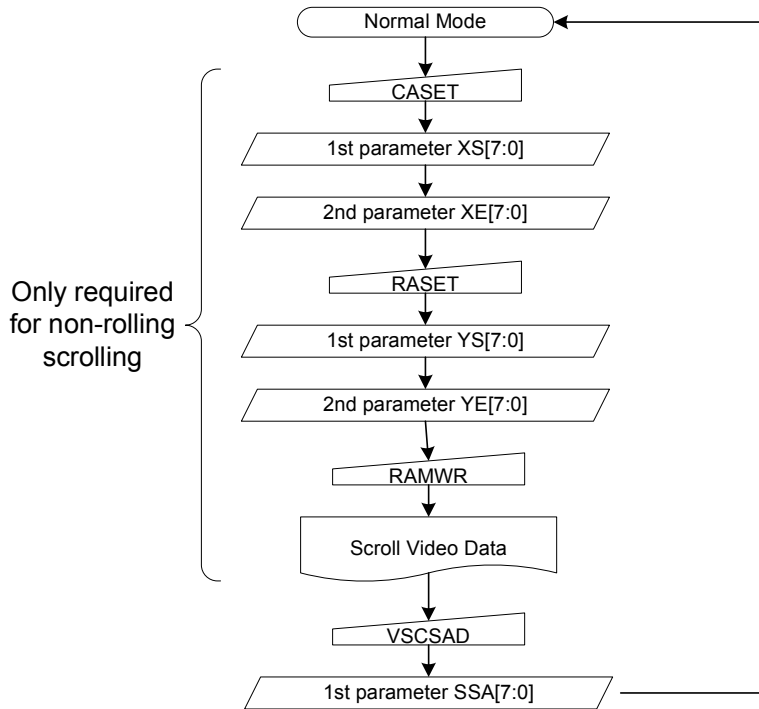
Description	<p>This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll.</p> <p>When MADCTR ML=0</p> <p>The 1st parameter TFA [7:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).</p> <p>The 2nd parameter VSA [7:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area.</p> <p>The 3rd parameter BFA [7:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).</p> <p>TFA, VSA and BFA refer to the Frame Memory Line Pointer.</p>	
Restriction	The condition is (TFA+VSA+BFA) = 132, otherwise Scrolling mode is undefined.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value		
		TFA [7:0]	VSA [7:0]	BFA [7:0]
	Power On Sequence	00h	84h	00h
	S/W Reset	00h	84h	00h
	H/W Reset	00h	84h	00h

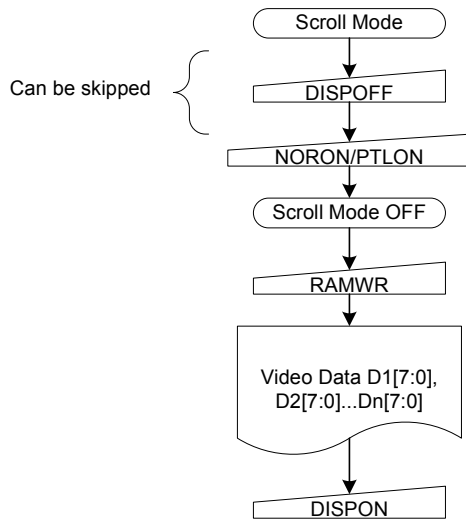


Flow Chart

2. Continuous Scroll:



3. To Exit Vertical Scroll Mode:



NOTE: Scroll Mode can be exit by both the Normal Display Mode On(13h) and Partial Mode On (12h) commands.

ST7637

9.1.29. TEOFF: Tearing Effect Line OFF (34h)

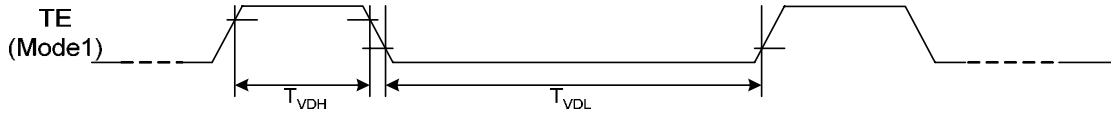
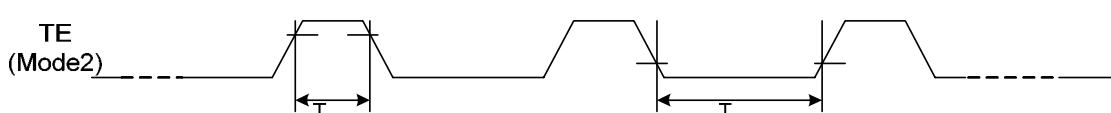
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEOFF	0	1	0	0	0	1	1	0	1	0	0	(34h)
Parameter	No Parameter											

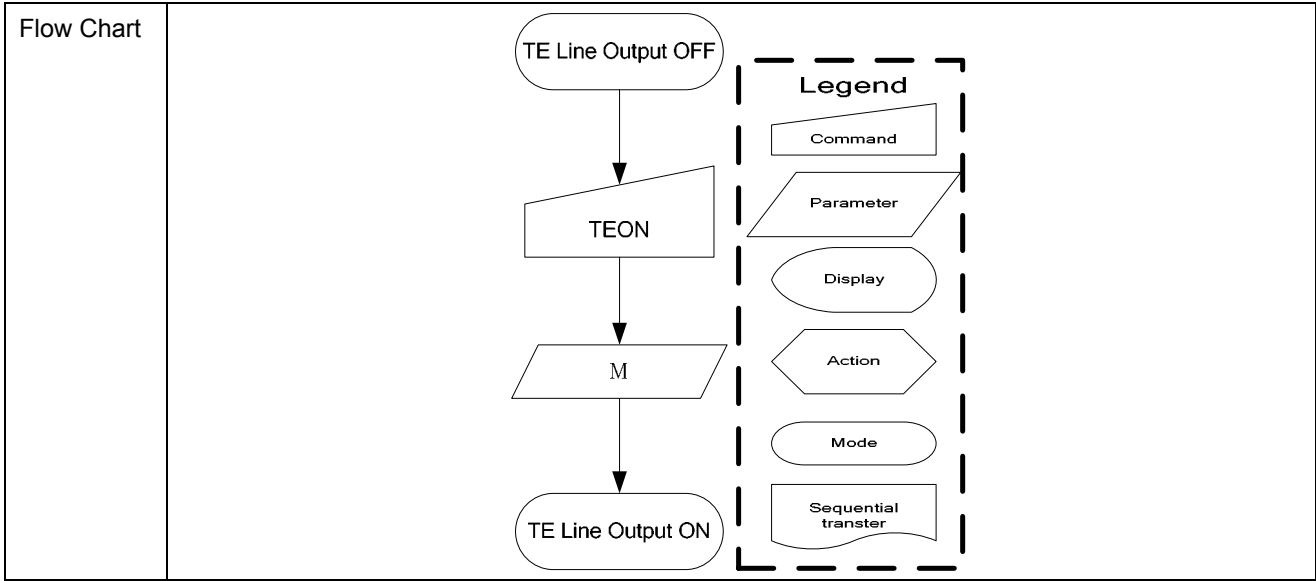
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.	
Restriction	This command has no effect when Tearing Effect output is already OFF.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	Tearing effect off
	S/W Reset	Tearing effect off
	H/W Reset	Tearing effect off
Flow Chart	<pre> graph TD A([TE Line Output ON]) --> B[/TEOFF/] B --> C([TE Line Output OFF]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Trapezoid Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Rounded rectangle Sequential transfer: Wavy rectangle 	

9.1.30. TEON: Tearing Effect Line ON (35h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEON	0	1	0	0	0	1	1	0	1	0	1	(35h)
Parameter	1	1	0	-	-	-	-	-	-	-	M	

NOTE: “-“ Don't care

Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTR bit ML.</p> <p>The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. (“-“=Don't Care).</p> <p>When M=0:</p> <p>The Tearing Effect Output Line consists of V-Blanking information only:</p>  <p>When M=1:</p> <p>The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p>  <p>See section 7.4.8 for more information.</p> <p><i>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</i></p>	
	Restriction	This command has no effect when Tearing Effect output is already OFF.
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	Tearing effect off & M=0
	S/W Reset	Tearing effect off & M=0
	H/W Reset	Tearing effect off & M=0



9.1.31. MADCTR: Memory Data Access Control (36h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
MADCTR	0	1	0	0	0	1	1	0	1	1	0	(36h)
Parameter	1	1	0	MY	MX	MV	ML	RGB	-	-	-	-

NOTE: “-“ Don't care

Description	<p>This command defines read/write scanning direction of frame memory.</p> <p>This command makes no change on the other driver status.</p> <p>Note: ML affects to Partial Area (30h), Vertical Scrolling Definition (33h), Vertical Scrolling Start address (37h), Partial On (12h) commands</p>																
	<p style="text-align: center;">Bit Assignment</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>NAME</th> <th>DESCRIPTION</th> </tr> </thead> <tbody> <tr> <td>MY</td> <td>ROW ADDRESS ORDER</td> <td rowspan="3">These 3bits controls MCU to memory write/read direction.</td> </tr> <tr> <td>MX</td> <td>COLUMN ADDRESS ORDER</td> </tr> <tr> <td>MV</td> <td>ROW/COLUMN ORDER</td> </tr> <tr> <td>ML</td> <td>LINE ADDRESS ORDER</td> <td>LCD refresh direction control</td> </tr> <tr> <td>RGB</td> <td>RGB-BGR ORDER</td> <td>Color selector switch control 0=RGB color filter panel, 1=BGR color filter panel) The contents of the frame memory are not changed.</td> </tr> </tbody> </table>		Bit	NAME	DESCRIPTION	MY	ROW ADDRESS ORDER	These 3bits controls MCU to memory write/read direction.	MX	COLUMN ADDRESS ORDER	MV	ROW/COLUMN ORDER	ML	LINE ADDRESS ORDER	LCD refresh direction control	RGB	RGB-BGR ORDER
Bit	NAME	DESCRIPTION															
MY	ROW ADDRESS ORDER	These 3bits controls MCU to memory write/read direction.															
MX	COLUMN ADDRESS ORDER																
MV	ROW/COLUMN ORDER																
ML	LINE ADDRESS ORDER	LCD refresh direction control															
RGB	RGB-BGR ORDER	Color selector switch control 0=RGB color filter panel, 1=BGR color filter panel) The contents of the frame memory are not changed.															
Restriction	D2, D1 and D0 of the 1st parameter are set to '000' internally.																
Register Availability	Status	Availability															
	Normal Mode On, Idle Mode Off, Sleep Out	Yes															

ST7637

	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0	
	S/W Reset	Not changed	
	H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0	
Flow Chart	<p>The flow chart shows a trapezoidal symbol labeled 'MADCTR' with an arrow pointing down to a parallelogram symbol labeled '1st parameter' with the subtext 'MX,MY,MV,ML,RGB'. To the right is a legend box containing six symbols: a trapezoid for 'Command', a parallelogram for 'Parameter', an oval for 'Display', a hexagon for 'Action', a rounded rectangle for 'Mode', and a wavy rectangle for 'Sequential transfer'.</p>		

9.1.32. VSCSAD: Vertical Scroll Start Address of RAM (37h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VSCSAD	0	1	0	0	0	1	1	0	1	1	1	(37h)
Parameter	1	1	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.

The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

This command Start the scrolling.

Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).

When MADCTR ML=0

Example:

When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=132 and Vertical Scrolling Pointer SSA='3'.

When MADCTR ML=1

Example:

When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=132 and Vertical Scrolling Pointer SSA='3'.

NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

SSA refers to the Frame Memory line Pointer.

ST7637

Restriction	<p>Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.</p> <p>SSA [7:0] is based on line unit.</p> <p>SSA [6:0] = 00h, 01h, 02h, 03h, ... , 83h</p>	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	No
	Partial Mode On, Idle Mode On, Sleep Out	No
	Sleep In	Yes
Default	Status	Default Value (SSA[7:0])
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	See Vertical Scrolling Definition (33h) description.	

9.1.33. IDMOFF: Idle Mode Off (38h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
IDMOFF	0	1	0	0	0	1	1	1	0	0	0	(38h)
Parameter	No Parameter											

Description	<p>This command is used to recover from Idle mode on.</p> <p>There will be no abnormal visible effect on the display mode change transition.</p> <p>In the idle off mode,</p> <ol style="list-style-type: none"> LCD can display maximum 262,144 colors. Normal frame frequency is applied. 	
Restriction	This command has no effect when module is already in idle off mode.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	Idle mode off
	S/W Reset	Idle mode off
	H/W Reset	Idle mode off
Flow Chart	<pre> graph TD A([Idle on mode]) --> B[/IDMOFF/] B --> C([Idle off mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Trapezoid Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Rounded rectangle Sequential transfer: Wavy line 	

9.1.34. IDMON: Idle Mode On (39h)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
IDMON	0	1	0	0	0	1	1	1	0	0	1	(39h)
Parameter	No Parameter											

Description	<p>This command is used to enter into Idle mode on.</p> <p>There will be no abnormal visible effect on the display mode change transition. In the idle on mode,</p> <ol style="list-style-type: none"> Color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed. 8-Color mode frame frequency is applied. Exit from IDMON by Idle Mode Off (38h) command <p>(Example)</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Memory</p> </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>Display</p> </div> </div> <p style="text-align: right;">“X”: don't care</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Color</th> <th>R5 R4 R3 R2 R1 R0</th> <th>G5 G4 G3 G2 G1 G0</th> <th>B5 B4 B3 B2 B1 B0</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Blue</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Red</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Magenta</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Green</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Cyan</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Yellow</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>White</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> </tbody> </table>			Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0	Black	0XXXXX	0XXXXX	0XXXXX	Blue	0XXXXX	0XXXXX	1XXXXX	Red	1XXXXX	0XXXXX	0XXXXX	Magenta	1XXXXX	0XXXXX	1XXXXX	Green	0XXXXX	1XXXXX	0XXXXX	Cyan	0XXXXX	1XXXXX	1XXXXX	Yellow	1XXXXX	1XXXXX	0XXXXX	White	1XXXXX	1XXXXX	1XXXXX
	Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0																																			
Black	0XXXXX	0XXXXX	0XXXXX																																				
Blue	0XXXXX	0XXXXX	1XXXXX																																				
Red	1XXXXX	0XXXXX	0XXXXX																																				
Magenta	1XXXXX	0XXXXX	1XXXXX																																				
Green	0XXXXX	1XXXXX	0XXXXX																																				
Cyan	0XXXXX	1XXXXX	1XXXXX																																				
Yellow	1XXXXX	1XXXXX	0XXXXX																																				
White	1XXXXX	1XXXXX	1XXXXX																																				
Restriction	This command has no effect when module is already in idle on mode.																																						
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																								
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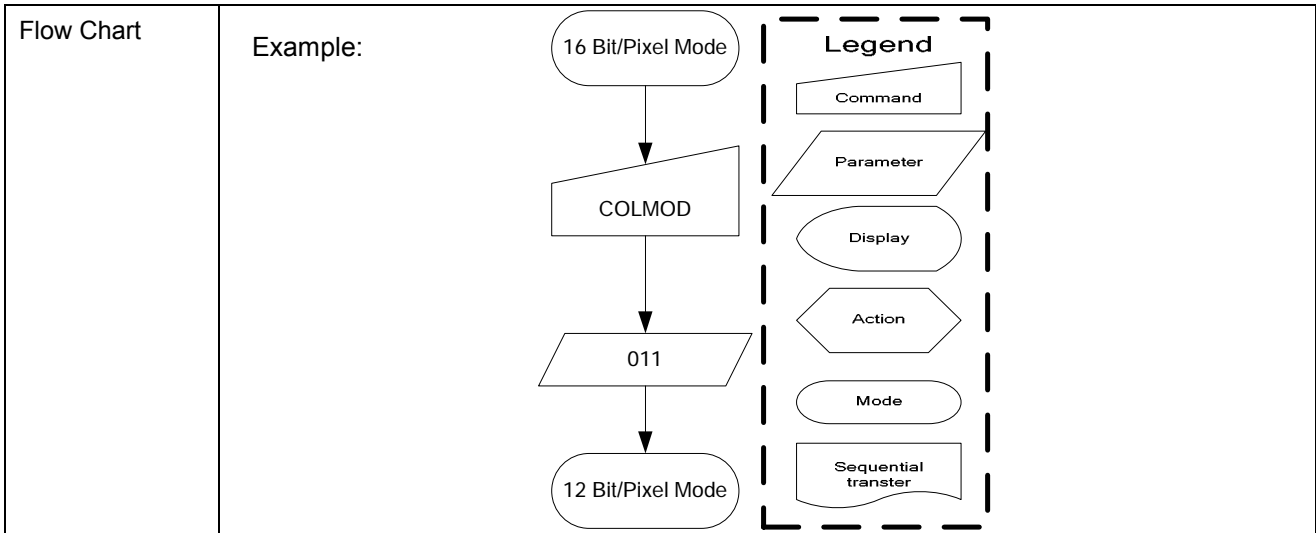
ST7637

Default	Status	Default Value
	Power On Sequence	Idle mode off
	S/W Reset	Idle mode off
	H/W Reset	Idle mode off
Flow Chart	<pre>graph TD; A([Idle off mode]) --> B[/IDMON/]; B --> C([Idle on mode]);</pre> <p>Legend</p> <ul style="list-style-type: none">Command: TrapezoidParameter: ParallelogramDisplay: OvalAction: HexagonMode: Rounded rectangleSequential transfer: Wavy rectangle	

9.1.35. COLMOD: Interface Pixel Format (3Ah)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
COLMOD	0	1	0	0	0	1	1	1	0	1	0	(3Ah)
Parameter	1	1	0	-	-	-	-	-	P2	P1	P0	-

Description	This command is used to define the format of RGB picture data, which is to be transferred via the MCU Interface. The formats are shown in the table:	
	Interface Format	P2 P1 P0
	Not Defined	0 0 0
	Not Defined	0 0 1
	8Bit/Pixel	0 1 0
	12Bit/Pixel (Type A)	0 1 1
	12Bit/Pixel (Type B)	1 0 0
	16Bit/Pixel	1 0 1
	18Bit/Pixel	1 1 0
	24Bit/Pixel	1 1 1
<i>Note: In 8 bit/pixel, 12bit/pixel or 16 bit/pixel mode, the LUT is applied to transfer data into the Frame Memory.</i>		
Restriction	There is no visible effect until the Frame Memory is written to.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	05h (16Bit/Pixel)
	S/W Reset	No Change
	H/W Reset	05h (16Bit/Pixel)



9.1.36. RDID1: Read ID1 Value (DAh)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID1	0	1	0	1	1	0	1	1	0	1	0	(DAh)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2 nd parameter	1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-

NOTE: “-“ Don't care

Description	This read byte returns 8-bit LCD module's manufacturer ID D7-D0 (ID17 to ID10): LCD module's manufacturer ID. NOTE: See command RDDID (04h), 2 nd parameter.	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	Not fixed
	S/W Reset	Not fixed
	H/W Reset	Not fixed
Flow Chart		

9.1.37. RDID2: Read ID2 Value (DBh)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID2	0	1	0	1	1	0	1	1	0	1	1	(DBh)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: “-“ Don't care

Description	<p>This read byte returns 8-bit LCD module/driver version ID D7-D0 (ID27 to ID20): LCD module/driver version ID Parameter Range: ID=80h to FFh NOTE: See command RDDID (04h), 3rd parameter.</p>													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Not fixed</td> </tr> <tr> <td>S/W Reset</td> <td>Not fixed</td> </tr> <tr> <td>H/W Reset</td> <td>Not fixed</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Not fixed	S/W Reset	Not fixed	H/W Reset	Not fixed					
Status	Default Value													
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H/W Reset	Not fixed													
Flow Chart														

9.1.38. RDID3: Read ID3 Value (DCh)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID3	0	1	0	1	1	0	1	1	1	0	0	(DCh)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: “-“ Don't care

Description	This read byte returns 8-bit LCD module/driver ID. D7-D0 (ID37 to ID30): LCD module/driver ID. NOTE: See command RDDID (04h), 4th parameter.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Not fixed</td> </tr> <tr> <td>S/W Reset</td> <td>Not fixed</td> </tr> <tr> <td>H/W Reset</td> <td>Not fixed</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Not fixed	S/W Reset	Not fixed	H/W Reset	Not fixed					
Status	Default Value													
Power On Sequence	Not fixed													
S/W Reset	Not fixed													
H/W Reset	Not fixed													
Flow Chart														

9.1.39. DutySet: Display Duty setting (B0H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DutySet	0	1	0	1	0	1	1	0	0	0	0	(B0h)
Parameter	1	1	0	Du7	Du6	Du5	Du4	Du3	Du2	Du1	Du0	-

NOTE: “-“ Don't care

Description	This command is used to set display duty. Command set = display duty numbers - 1.																														
	Example: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Duty</th> <th>Du7</th> <th>Du6</th> <th>Du5</th> <th>Du4</th> <th>Du3</th> <th>Du2</th> <th>Du1</th> <th>Du0</th> <th>Command set=</th> </tr> </thead> <tbody> <tr> <td>Example: 1/132 duty</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>Display duty numbers-1 132-1=131</td> </tr> </tbody> </table>												Duty	Du7	Du6	Du5	Du4	Du3	Du2	Du1	Du0	Command set=	Example: 1/132 duty	1	0	0	0	0	0	1	1
Duty	Du7	Du6	Du5	Du4	Du3	Du2	Du1	Du0	Command set=																						
Example: 1/132 duty	1	0	0	0	0	0	1	1	Display duty numbers-1 132-1=131																						
Restriction	Display duty must > 4 (1/4 duty)																														
Register Availability	Status						Availability																								
	Normal Mode On, Idle Mode Off, Sleep Out						Yes																								
	Normal Mode On, Idle Mode On, Sleep Out						Yes																								
	Partial Mode On, Idle Mode Off, Sleep Out						Yes																								
	Partial Mode On, Idle Mode On, Sleep Out						Yes																								
	Sleep In						Yes																								
Default	Status						Default Value (Du[7:0])																								
	Power On Sequence						10000011b (83h)																								
	S/W Reset						10000011b (83h)																								
	H/W Reset						10000011b (83h)																								
Flow Chart	<pre> graph TD DutySet[Command] --> Du7_0[/Parameter Du[7:0]/] </pre> <p>The flow chart illustrates the execution of the DutySet command. It starts with a rectangular box labeled 'DutySet', which is identified in the legend as a 'Command'. An arrow points from this box to a parallelogram box labeled 'Du[7:0]', identified in the legend as a 'Parameter'. To the right of the flow chart is a legend enclosed in a dashed box, defining the symbols used: a rectangle for 'Command', a parallelogram for 'Parameter', an oval for 'Display', a hexagon for 'Action', another oval for 'Mode', and a cloud-like shape for 'Sequential transfer'.</p>																														

9.1.40. FirstCom: First Com. Page address (B1H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
FirstCom	0	1	0	1	0	1	1	0	0	0	1	(B1h)
Parameter	1	1	0	F7	F6	F5	F4	F3	F2	F1	F0	-

NOTE: “-“ Don't care

Description	This command defines the first output COM number that mapping to the RAM page address 0. For detail setting value, please see the table as below.																																																															
	<table border="1"> <thead> <tr> <th>F7</th> <th>F6</th> <th>F5</th> <th>F4</th> <th>F3</th> <th>F2</th> <th>F1</th> <th>F0</th> <th>Line address</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td></td> <td></td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td></td> <td></td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td></td> <td></td> <td>0</td> <td>2</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td></td> <td></td> <td>1</td> <td>3</td> </tr> <tr> <td>0</td> <td>:</td> <td>:</td> <td>:</td> <td>:</td> <td></td> <td></td> <td>:</td> <td>:</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>131</td> </tr> </tbody> </table>		F7	F6	F5	F4	F3	F2	F1	F0	Line address	0	0	0	0	0			0	0	0	0	0	0	0			1	1	0	0	0	0	1			0	2	0	0	0	0	1			1	3	0	:	:	:	:			:	:	1	0	0	0	0	0	1	1
F7	F6	F5	F4	F3	F2	F1	F0	Line address																																																								
0	0	0	0	0			0	0																																																								
0	0	0	0	0			1	1																																																								
0	0	0	0	1			0	2																																																								
0	0	0	0	1			1	3																																																								
0	:	:	:	:			:	:																																																								
1	0	0	0	0	0	1	1	131																																																								
Example: If FirstCom=8, common 8 would output the data of RAM page address 0.																																																																
Restriction																																																																
Register Availability	Status	Availability																																																														
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																														
	Normal Mode On, Idle Mode On, Sleep Out	Yes																																																														
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																																																														
	Partial Mode On, Idle Mode On, Sleep Out	Yes																																																														
	Sleep In	Yes																																																														
Default	Status	Default Value (F[7:0])																																																														
	Power On Sequence	00h																																																														
	S/W Reset	00h																																																														
	H/W Reset	00h																																																														
Flow Chart	<pre> graph TD FirstCom[FirstCom] --> F7_0[/F[7:0]/] </pre>																																																															

9.1.41. OscDiv: FOSC Divider (B3H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
OscDiv	0	1	0	1	0	1	1	0	0	1	1	(B3h)
Parameter	1	1	0	-	-	-	-	-	-	CLD1	CLD0	-

NOTE: “-“ Don't care

Description	<p>This command is used to specify the CL dividing ratio.</p> <p>CLD1, CLD0: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>CLD1</th> <th>CLD0</th> <th>CL dividing ratio</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Not divide</td> </tr> <tr> <td>0</td> <td>1</td> <td>2 divisions</td> </tr> <tr> <td>1</td> <td>0</td> <td>4 divisions</td> </tr> <tr> <td>1</td> <td>1</td> <td>8 divisions</td> </tr> </tbody> </table>			CLD1	CLD0	CL dividing ratio	0	0	Not divide	0	1	2 divisions	1	0	4 divisions	1	1	8 divisions
CLD1	CLD0	CL dividing ratio																
0	0	Not divide																
0	1	2 divisions																
1	0	4 divisions																
1	1	8 divisions																
Restriction																		
Register Availability	Status	Availability																
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																
	Normal Mode On, Idle Mode On, Sleep Out	Yes																
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																
	Partial Mode On, Idle Mode On, Sleep Out	Yes																
	Sleep In	Yes																
Default	Status	Default Value (CLD[0:1])																
	Power On Sequence	00b																
	S/W Reset	00b																
	H/W Reset	00b																
Flow Chart	<p>The flow chart shows a trapezoidal box labeled 'OscDiv' with a downward arrow pointing to a parallelogram box labeled 'CLD[2:0]'. To the right, a dashed box contains a legend with the following items: Command (trapezoid), Parameter (parallelogram), Display (oval), Action (hexagon), Mode (rounded rectangle), and Sequential transfer (dashed box).</p>																	

9.1.42. NLInvSet: N-Line control (B5H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NLInvSet	0	1	0	1	0	1	1	0	1	0	1	(B5h)
Parameter	1	1	0	M	N6	N5	N4	N3	N2	N1	N0	-

NOTE: “-“ Don't care

Description	<p>This command is used to set the inverted line number with range of 2 to (duty-1) to improve display quality. When M=0, inversion occurs in every frame; when M=1, inversion is independent from frames. If N[6:0]=0, N-line inversion function is disable.</p> <p>Line inversion numbers=N[6:0] +1.</p> <p>Example: If N[6:0]=7, inversion occurs per 8 line.</p>															
Restriction																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
Normal Mode On, Idle Mode On, Sleep Out	Yes															
Partial Mode On, Idle Mode Off, Sleep Out	Yes															
Partial Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>M</th> <th>N[6:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0b</td> <td>0000000b</td> </tr> <tr> <td>S/W Reset</td> <td>0b</td> <td>0000000b</td> </tr> <tr> <td>H/W Reset</td> <td>0b</td> <td>0000000b</td> </tr> </tbody> </table>		Status	Default Value		M	N[6:0]	Power On Sequence	0b	0000000b	S/W Reset	0b	0000000b	H/W Reset	0b	0000000b
Status	Default Value															
	M	N[6:0]														
Power On Sequence	0b	0000000b														
S/W Reset	0b	0000000b														
H/W Reset	0b	0000000b														
Flow Chart	<pre> graph TD NLInvSet[Command] --> M[Parameter] M --> N60[Parameter] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Trapezoid Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Rounded rectangle Sequential transfer: Wavy rectangle 															

9.1.43. ComScanDir: Com/Seg Scan Direction for glass layout (B7H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
ComScanDir	0	1	0	1	0	1	1	0	1	1	1	(B7h)
Parameter	1	1	0	0	SMX	0	0	SBGR	0	0	0	-

NOTE: “-“ Don’t care

Description	Function		0	1
	SMX	Inverse the MX setting	Keep MX	Inverse MX
	SBGR	Inverse the BGR setting	Keep BGR	Inverse BGR
Restriction				
Register Availability	Status	Availability		
	Normal Mode On, Idle Mode Off, Sleep Out	Yes		
	Normal Mode On, Idle Mode On, Sleep Out	Yes		
	Partial Mode On, Idle Mode Off, Sleep Out	Yes		
	Partial Mode On, Idle Mode On, Sleep Out	Yes		
	Sleep In	Yes		
Default	Status	Default Value		
	Power On Sequence	000b		
	S/W Reset	000b		
	H/W Reset	000b		
Flow Chart	<pre> graph TD A[ComScanDir] --> B[/CSD[2:0]/] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 			

ST7637

9.1.44. RMWIN: Read Modify Write control IN (B8H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RMWIN	0	1	0	1	0	1	1	1	0	0	0	(B8h)
Parameter	No Parameter											

NOTE: “-“ Don't care

Description	Read modify write control IN	
Restriction		
Register	Status	Availability
Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	--
	S/W Reset	--
	H/W Reset	--

ST7637

9.1.45. RMWOUT: Read Modify Write control out(B9H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RMWOUT	0	1	0	1	0	1	1	1	0	0	1	(B9h)
Parameter	No Parameter											

NOTE: “-“ Don't care

Description	Read modify write control OUT	
Restriction		
Register	Status	Availability
Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	--
	S/W Reset	--
	H/W Reset	--

9.1.46. VopSet: Vop set (C0H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VopSet	0	1	0	1	1	0	0	0	0	0	0	(C0h)
1 st parameter	1	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	-
2 nd parameter	1	1	0	-	-	-	-	-	-	-	Vop8	

NOTE: “-“ Don't care

Description	The command is used to program the optimum LCD supply voltage V0. Please see Section 7.10 for reference.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value (Vop=12V)	
		Vop8	Vop[7:0]
	Power On Sequence	0	11010010b (D2h)
	S/W Reset	0	11010010b (D2h)
	H/W Reset	0	11010010b (D2h)
Flow Chart	<pre> graph TD VopSet[VopSet] --> Param[1st & 2nd parameter Vop[8:0]] </pre> <p>The flow chart illustrates the execution of the VopSet command. It starts with a trapezoidal 'Command' box labeled 'VopSet'. An arrow points down to a parallelogram 'Parameter' box labeled '1st & 2nd parameter Vop[8:0]'. To the right, a dashed box contains a legend with six symbols: a trapezoid for 'Command', a parallelogram for 'Parameter', an oval for 'Display', a hexagon for 'Action', a rounded rectangle for 'Mode', and a wavy rectangle for 'Sequential transfer'.</p>		

9.1.47. VopOffsetInc: Vop Increase 1 (C1H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VopOffsetInc	0	1	0	1	1	0	0	0	0	0	1	(C1h)

NOTE: “-“ Don't care

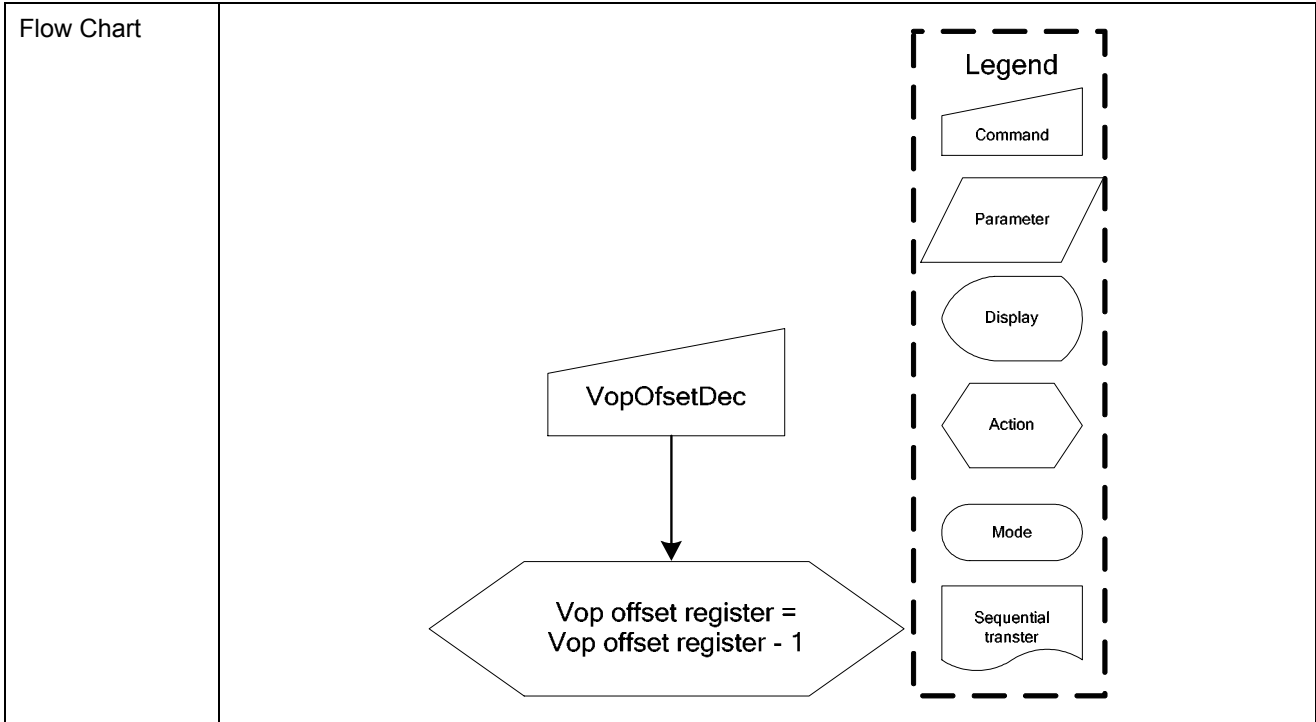
Description	<p>With the VopOffsetInc and VopOffsetDec command the V_{LC}D voltage and therewith the contrast of the LCD can be adjusted. This command increases the value of Vop offset register by 1.</p> <p>If you set the electronic control value to 1111111, the control value is set to 0000000 after this command has been executed.</p>	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	--
	S/W Reset	--
	H/W Reset	--
Flow Chart	<pre> graph TD A[VopOffsetInc] --> B{Vop offset register = Vop offset register + 1} </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Trapezoid Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Rounded rectangle Sequential transfer: Wavy rectangle 	

9.1.48. VopOffsetDec: Vop Decrease 1 (C2H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VopOffsetDec	0	1	0	1	1	0	0	0	0	1	0	(C2h)

NOTE: “-“ Don't care

Description	<p>With the VopOffsetInc and VopOffsetDec command the V_{LC}D voltage and therewith the contrast of the LCD can be adjusted. This command decreases the value of Vop offset register by 1.</p> <p>If you set the electronic control value to 0000000, the control value is set to 1111111 after this command has been executed.</p>																																										
	<table border="1"> <thead> <tr> <th>Electronic Control Value</th> <th>Decimal Equivalent</th> <th>V0 Offset</th> </tr> </thead> <tbody> <tr> <td>0111111</td> <td>63</td> <td>+2520 mV</td> </tr> <tr> <td>0111110</td> <td>62</td> <td>+2480 mV</td> </tr> <tr> <td>0111101</td> <td>61</td> <td>+2440 mV</td> </tr> <tr> <td>...</td> <td>...</td> <td>...</td> </tr> <tr> <td>0000010</td> <td>2</td> <td>+80 mV</td> </tr> <tr> <td>0000001</td> <td>1</td> <td>+40 mV</td> </tr> <tr> <td>0000000</td> <td>0</td> <td>0 mV</td> </tr> <tr> <td>1111111</td> <td>-1</td> <td>-40 mV</td> </tr> <tr> <td>1111110</td> <td>-2</td> <td>-80 mV</td> </tr> <tr> <td>...</td> <td>...</td> <td>...</td> </tr> <tr> <td>1100010</td> <td>-62</td> <td>-2480 mV</td> </tr> <tr> <td>1100001</td> <td>-63</td> <td>-2520 mV</td> </tr> <tr> <td>1100000</td> <td>-64</td> <td>-2560mV</td> </tr> </tbody> </table> <p style="text-align: center;">Table 9.1-1 Possible Vop[6:0] values</p>		Electronic Control Value	Decimal Equivalent	V0 Offset	0111111	63	+2520 mV	0111110	62	+2480 mV	0111101	61	+2440 mV	0000010	2	+80 mV	0000001	1	+40 mV	0000000	0	0 mV	1111111	-1	-40 mV	1111110	-2	-80 mV	1100010	-62	-2480 mV	1100001	-63	-2520 mV	1100000	-64
Electronic Control Value	Decimal Equivalent	V0 Offset																																									
0111111	63	+2520 mV																																									
0111110	62	+2480 mV																																									
0111101	61	+2440 mV																																									
...																																									
0000010	2	+80 mV																																									
0000001	1	+40 mV																																									
0000000	0	0 mV																																									
1111111	-1	-40 mV																																									
1111110	-2	-80 mV																																									
...																																									
1100010	-62	-2480 mV																																									
1100001	-63	-2520 mV																																									
1100000	-64	-2560mV																																									
Restriction																																											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																														
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>--</td> </tr> <tr> <td>S/W Reset</td> <td>--</td> </tr> <tr> <td>H/W Reset</td> <td>--</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	--	S/W Reset	--	H/W Reset	--																																		
Status	Default Value																																										
Power On Sequence	--																																										
S/W Reset	--																																										
H/W Reset	--																																										



9.1.49. BiasSel: Bias Selection (C3H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
BiasSel	0	1	0	1	1	0	0	0	0	1	1	(C3h)
Parameter	1	1	0	-	-	-	-	-	Bias2	Bias1	Bias0	-

NOTE: “-“ Don't care

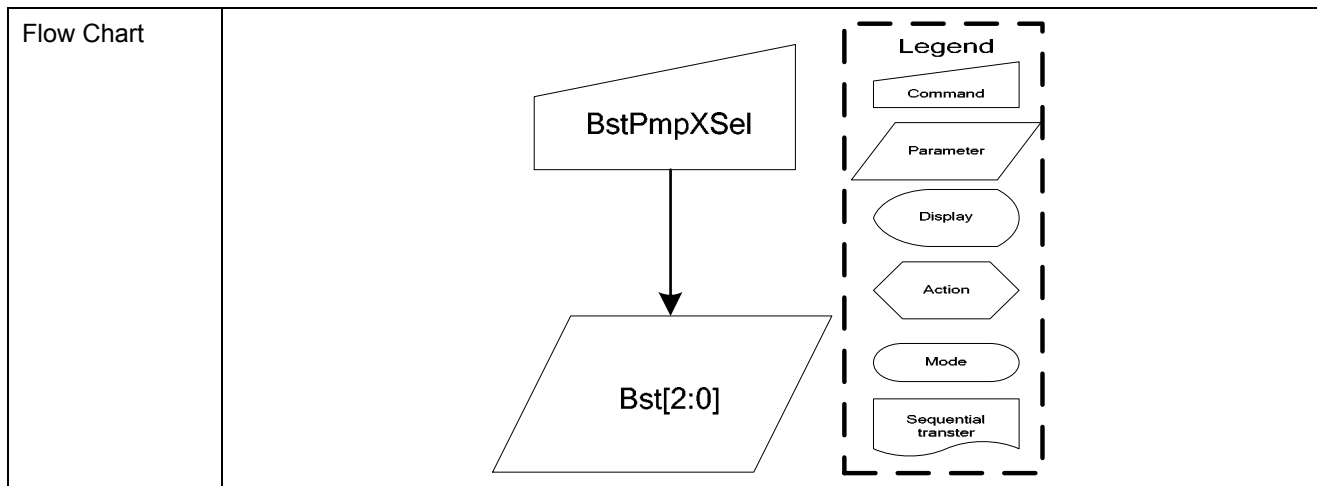
Description	Select LCD bias ratio of the voltage required for driving the LCD.			
	Bais2	Bais1	Bais0	LCD bias
	0	0	0	1/12
	0	0	1	1/11
	0	1	0	1/10
	0	1	1	1/9
	1	0	0	1/8
	1	0	1	1/7
	1	1	0	1/6
1	1	1	1/5	
Restriction				
Register Availability	Status	Availability		
	Normal Mode On, Idle Mode Off, Sleep Out	Yes		
	Normal Mode On, Idle Mode On, Sleep Out	Yes		
	Partial Mode On, Idle Mode Off, Sleep Out	Yes		
	Partial Mode On, Idle Mode On, Sleep Out	Yes		
	Sleep In	Yes		
Default	Status	Default Value (Bias[2:0])		
	Power On Sequence	110b		
	S/W Reset	110b		
	H/W Reset	110b		
Flow Chart	<pre> graph TD BiasSel[Command] --> BS[Parameter] </pre> <p>The flow chart illustrates the execution of the BiasSel command. The command is represented by a rectangle, and the resulting parameter BS[2:0] is represented by a parallelogram. A legend on the right defines the symbols used in the flow chart: a rectangle for Command, a parallelogram for Parameter, an oval for Display, a hexagon for Action, a rounded rectangle for Mode, and a wavy rectangle for Sequential transfer.</p>			

9.1.50. BstPmpXSel: Booster Setting (C4H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
BstPmpXSel	0	1	0	1	1	0	0	0	1	0	0	(C4h)
Parameter	1	1	0	-	-	-	-	-	BST2	BST 1	BST0	-

NOTE: “-“ Don't care

Description	Booster setting			
	BST2	BST1	BST0	
	0	0	0	x1 boosting circuit (Booster off)
	0	0	1	x2 boosting circuit
	0	1	0	x3 boosting circuit
	0	1	1	x4 boosting circuit
	1	0	0	x5 boosting circuit
	1	0	1	x6 boosting circuit
	1	1	0	x7 boosting circuit
	1	1	1	x8 boosting circuit
Restriction				
Register Availability	Status	Availability		
	Normal Mode On, Idle Mode Off, Sleep Out	Yes		
	Normal Mode On, Idle Mode On, Sleep Out	Yes		
	Partial Mode On, Idle Mode Off, Sleep Out	Yes		
	Partial Mode On, Idle Mode On, Sleep Out	Yes		
	Sleep In	Yes		
Default	Status	Default Value (BST[2:0])		
	Power On Sequence	110b		
	S/W Reset	110b		
	H/W Reset	110b		

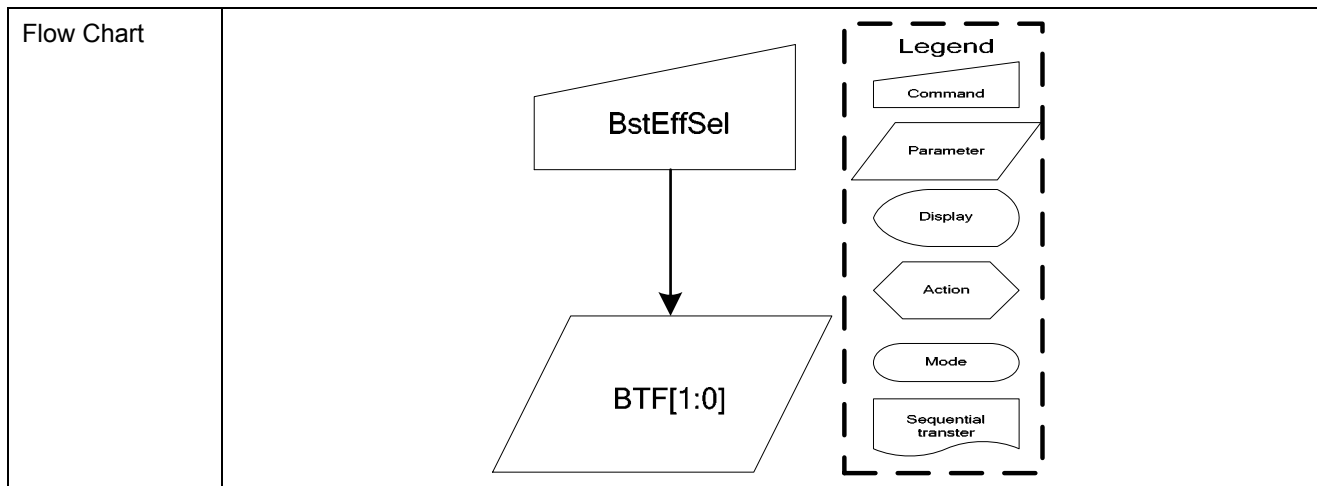


9.1.51. BstEffSel: Booster Efficiency selection (C5H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
BstEffSel	0	1	0	1	1	0	0	0	1	0	1	(C5h)
Parameter	1	1	0	-	-	-	-	-	-	BTF1	BTF0	-

NOTE: “-“ Don't care

Description	Booster Efficiency set		
	BTF1	BTF0	Frequency (Hz)
	0	0	Level 1
	0	1	Level 2 (default)
	1	0	Level 3
	By Booster Stages (2X, 3X, 4X, 5X, 6X, 7X, 8X) and Booster Efficiency (Level1~3) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level3 is higher than level1). The Boost Efficiency is better than lower level, and it just need few more power consumption current.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value (BTF[1:0])	
	Power On Sequence	01b	
	S/W Reset	01b	
	H/W Reset	01b	



9.1.52. VopOffset: Vop offset fuse bit adjust (C7H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VopOffset	0	1	0	1	1	0	0	0	1	1	1	(C7h)
Parameter1	1	1	0	VOS7	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0	-
Parameter2	1	1	0	-	-	-	-	-	-	-	VOS8	-

NOTE: “-“ Don't care

Description	The command is used to the Vop offset for V0.		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
		VOS8	VOS[7:0]
	Power On Sequence	0	0
	S/W Reset	0	0
	H/W Reset	0	0
Flow Chart	<pre> graph TD VopOffset[VopOffset] --> Param[1st & 2nd parameter VOS[8:0]] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle with slanted top Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Horizontal rounded rectangle Sequential transfer: Wave-bottom shape 		

9.1.53. VgSorSel: Vg source control (CBH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
V3SorSel	0	1	0	1	1	0	0	1	0	1	1	(CBh)
Parameter	1	1	0	-	-	-	-	-	-	-	2BT0	-

NOTE: “-“ Don't care

Description	2BT0=0: Vg source comes from VDD2 ; 2BT0=1: Vg source comes from 2-times charge pump.	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (2BT0)
	Power On Sequence	1
	S/W Reset	1
	H/W Reset	1
Flow Chart	<pre> graph TD VgSorSel[Command] --> 2BT0[/Parameter/] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command (trapezoid) Parameter (parallelogram) Display (oval) Action (hexagon) Mode (rounded rectangle) Sequential transfer (wavy rectangle) 	

9.1.54. ID1Set : ID1 setting (CCH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
ID1Set	0	1	0	1	1	0	0	1	1	0	0	(CCh)
Parameter	1	1	0	ID1_7	ID1_6	ID1_5	ID1_4	ID1_3	ID1_2	ID1_1	ID1_0	-

NOTE: “-“ Don't care

Description	ID1 setting for OPT program data input	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	<pre> graph TD ID1Set[Command: ID1Set] --> D7_0[/Parameter: D[7:0]/] </pre> <p>The flow chart illustrates the execution of the ID1Set command. The command, represented by a trapezoid, is sent to the device, which then outputs the parameter D[7:0], represented by a parallelogram. A legend on the right defines the symbols used in the flow chart: a trapezoid for Command, a parallelogram for Parameter, an oval for Display, a hexagon for Action, a rounded rectangle for Mode, and a wavy rectangle for Sequential transfer.</p>	

ST7637

9.1.55. ID2Set : ID2 setting (CDH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
ID2Set	0	1	0	1	1	0	0	1	1	0	1	(CDh)
Parameter	1	1	0	1	ID2_6	ID2_5	ID2_4	ID2_3	ID2_2	ID2_1	ID2_0	-

NOTE: “-“ Don't care

Description	ID2 setting for OPT program data input	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	<pre> graph TD ID2Set[Command] --> D6_0[/Parameter/] </pre> <p>The flow chart illustrates the ID2Set command (represented by a trapezoid) pointing to the D[6:0] parameter (represented by a parallelogram). A legend on the right defines the symbols used: Command (trapezoid), Parameter (parallelogram), Display (oval), Action (hexagon), Mode (rounded rectangle), and Sequential transfer (wavy rectangle).</p>	

9.1.56. ID3Set : ID3 setting (CEH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
ID3Set	0	1	0	1	1	0	0	1	1	1	0	(CEh)
Parameter	1	1	0	ID3_7	ID3_6	ID3_5	ID3_4	ID3_3	ID3_2	ID3_1	ID3_0	-

NOTE: “-“ Don't care

Description	ID3 setting for OPT program data input	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	<pre> graph TD ID3Set[Command] --> D7_0[/Parameter/] </pre> <p>The flow chart illustrates the ID3Set command. A trapezoidal command box labeled 'ID3Set' has a downward arrow pointing to a parallelogram parameter box labeled 'D[7:0]'. To the right, a dashed-line legend defines the symbols used: a trapezoid for 'Command', a parallelogram for 'Parameter', an oval for 'Display', a hexagon for 'Action', a rounded rectangle for 'Mode', and a wavy rectangle for 'Sequential transfer'.</p>	

9.1.57. NASET: Analog circuit setting (D0H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
AutoLoadSet	0	1	0	1	1	0	1	0	0	0	0	(D0h)
Parameter	1	1	0	0	0	0	1	1	1	0	1	(1Dh)

NOTE: “-“ Don't care

Description	Analog circuit setting. Such as follower selection, level shifter power mode selection.	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value D[7:0]
	Power On Sequence	1Dh
	S/W Reset	1Dh
	H/W Reset	1Dh
Flow Chart	<pre> graph TD ANASET[ANASET] --> 1DH[/1DH/] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Trapezoid Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Rounded rectangle Sequential transfer: Wavy rectangle 	

9.1.58. AutoLoadSet: mask rom data auto re-load control (D7H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
AutoLoadSet	0	1	0	1	1	0	1	0	1	1	1	(D7h)
Parameter	1	1	0	EXTE	OTPBE	-	ARD	1	1	1	1	-

NOTE: “-“ Don't care

Description	Mask rom data auto re-load control EXTE : External command enable (OTP input), 1: enable, 0: disable OTPBE: OTPB auto-read enable (OTP input, force disable when ARD=0) ARD : OTP auto recovery enable control, 1: Disable OTP auto recovery, 0: Enable OTP auto recovery													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default ValueD[7:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default ValueD[7:0]	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default ValueD[7:0]													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	<p>The flow chart illustrates the execution of the AutoLoadSet command. A rectangular box labeled 'AutoLoadSet' has a downward arrow pointing to a parallelogram box labeled 'D[7](EXTE), D[4](ARD)'. To the right, a dashed-line legend defines the symbols used: a rectangle for 'Command', a parallelogram for 'Parameter', an oval for 'Display', a hexagon for 'Action', a rounded rectangle for 'Mode', and a wavy rectangle for 'Sequential transfer'.</p>													

9.1.59. RDTstStatus: Read IC status (DEH)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDTstStatus	0	1	0	1	1	0	1	1	1	1	0	(DEh)
Dummy Read	1	0	1	-	-	-	-	-	-	-	-	
Parameter	1	0	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	-

NOTE: "- " Don't care

Description	Read IC status. Contect of OTP / RDA / PWR_VOP read control (selection Byte by StusOutByteSel[3:0] control)		
Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	-	
	S/W Reset	-	
	H/W Reset	-	
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p> </div> </div> <div style="text-align: right; margin-top: 10px;"> <p>Host Display</p> </div> <div style="border: 1px dashed black; padding: 10px; margin-top: 20px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>		

9.1.60. EPCTIN: Control OTP WR/XRD (E0H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
EPCTIN	0	1	0	1	1	1	0	0	0	0	0	(E0h)
Parameter	1	1	0	0	0	WR /XRD	0	0	0	0	0	-

NOTE: “-“ Don't care

Description	WR/XRD: when setting “1” → The Write Enable of OTP will be opened. WR/XRD: when setting “0” → The Read Enable of OTP will be opened.	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (WR/XRD)
	Power On Sequence	0
	S/W Reset	0
	H/W Reset	0
Flow Chart	<pre> graph TD EPCTIN[EPCTIN] --> WRXRD[/WR/XRD/] </pre> <p>The flow chart illustrates the relationship between the EPCTIN command and the WR/XRD parameter. The EPCTIN command is represented by a trapezoid, and the WR/XRD parameter is represented by a parallelogram. An arrow points from the EPCTIN command to the WR/XRD parameter. A legend on the right side of the chart defines the symbols used: Command (trapezoid), Parameter (parallelogram), Display (oval), Action (hexagon), Mode (rounded rectangle), and Sequential transfer (dashed box).</p>	

ST7637

9.1.61. EPCOUT: OTP control cancel (E1H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
EPCOUT	0	1	0	1	1	1	0	0	0	0	1	(E1h)

NOTE: “-“ Don't care

Description	IC exits the OTP control circuit when executing this command.	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	--
	S/W Reset	--
	H/W Reset	--
Flow Chart	<pre> graph TD OTPSEL[/OTPSEL/] --> MS[MS[1:0]] MS --> EPCTIN[/EPCTIN/] EPCTIN --> WR[WR/XRD=1] WR --> EPMWR[/EPMWR/] EPMWR --> EPCOUT[/EPCOUT/] </pre>	

ST7637

9.1.62. EPMWR: Write to OTP (E2H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
EPCOUT	0	1	0	1	1	1	0	0	0	1	0	(E2h)

NOTE: “-“ Don't care

Description	IC activates trigger to start OTP programming when executing this command.	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	--
	S/W Reset	--
	H/W Reset	--
Flow Chart	<pre> graph TD OTPSEL[/OTPSEL/] --> MS[MS[1:0]] MS --> EPCTIN[/EPCTIN/] EPCTIN --> WR[WR/XRD=1] WR --> EPMWR[/EPMWR/] EPMWR --> EPCOUT[/EPCOUT/] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Parallelogram Parameter: Trapezoid Display: Oval Action: Hexagon Mode: Rounded rectangle Sequential transfer: Dashed line 	

ST7637

9.1.63. EPMRD: Read from OTP (E3H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
EPMRD	0	1	0	1	1	1	0	0	0	1	1	(E3h)

NOTE: “-“ Don't care

Description	IC activates trigger to start OTP data download to circuit when executing this command.	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	
	S/W Reset	
	H/W Reset	
Flow Chart	<pre> graph TD A[/OTPSEL/] --> B[MS[1:0]] B --> C[/EPCTIN/] C --> D[WR/XRD=1] D --> E[/EPMWR/] E --> F[/EPCOUT/] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Parallelogram Parameter: Trapezoid Display: Oval Action: Hexagon Mode: Rounded rectangle Sequential transfer: Wavy arrow 	

9.1.64. OTPSEL: OTP selection (E4H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
OTPSEL	0	1	0	1	1	1	0	0	1	0	0	(E4h)
Parameter	1	1	0	MS1	MS0	0	1	1	0	0	0	-

NOTE: “-“ Don't care

Description	This command defines OTP/OTPA/OTPB selection for EEPROM control. Please see the table as below:																
	<table border="1"> <thead> <tr> <th>MS1</th> <th>MS0</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Disable</td> </tr> <tr> <td>0</td> <td>1</td> <td>OTP</td> </tr> <tr> <td>1</td> <td>0</td> <td>OTPA</td> </tr> <tr> <td>1</td> <td>1</td> <td>OTPB</td> </tr> </tbody> </table>		MS1	MS0	Mode	0	0	Disable	0	1	OTP	1	0	OTPA	1	1	OTPB
MS1	MS0	Mode															
0	0	Disable															
0	1	OTP															
1	0	OTPA															
1	1	OTPB															
Restriction																	
Register Availability	Status	Availability															
	Normal Mode On, Idle Mode Off, Sleep Out	Yes															
	Normal Mode On, Idle Mode On, Sleep Out	Yes															
	Partial Mode On, Idle Mode Off, Sleep Out	Yes															
	Partial Mode On, Idle Mode On, Sleep Out	Yes															
	Sleep In	Yes															
Default	Status	Default Value (MS[1:0])															
	Power On Sequence	00															
	S/W Reset	00															
	H/W Reset	00															
Flow Chart	<pre> graph TD A[/OTPSEL/] --> B[MS[1:0]] B --> C[/EPCTIN/] C --> D[WR/XRD=1] D --> E[/EPMWR/] E --> F[/EPCOUT/] </pre>																

9.1.65. ROMSET: Programmable rom setting (E5H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
AutoLoadSet	0	1	0	0	1	1	1	0	1	0	1	(E5h)
Parameter	1	1	0	0	0	0	0	1	1	0	0	(0Ch)

NOTE: “-“ Don't care

Description	Set the OTP writing timing. Value 0x0C is the best value for ST7637.	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value D[7:0]
	Power On Sequence	0Fh
	S/W Reset	0Fh
	H/W Reset	0Fh
Flow Chart	<pre> graph TD ROMSET[ROMSET] --> 0CH[/0Ch/] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle with top-left corner cut off Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Horizontal rounded rectangle Sequential transfer: Wavy-bottom rectangle 	

9.1.66. LVMS: Low voltage mode Setting (E7H & E8H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command 1	0	1	0	1	1	1	0	0	1	1	1	(E7h)
1st parameter	1	1	0	0	0	1	0	0	0	1	0	(22h)
Command 2	0	1	0	1	1	1	0	1	0	0	0	(E8h)
1st parameter	1	1	0	0	0	1	1	0	1	1	1	(37h)
2nd parameter	1	1	0	0	0	0	0	0	0	1	0	(03h)
3rd parameter	1	1	0	0	0	0	1	1	1	1	1	(1Fh)

Description	Low voltage mode setting.																											
Restriction																												
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Sleep In	Yes																											
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Status	Default Value																											
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S/W Reset	12h	36h	03h	16h																								
H/W Reset	12h	36h	03h	16h																								
Flow Chart																												

9.1.67. HPMSET : High Power Mode Setting (EBH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	0	1	0	1	1	(Ebh)
1st parameter	1	1	0	0	0	0	0	0	0	1	0	(02h)
2nd parameter	1	1	0	0	0	0	0	0	0	0	1	(01h)

Description	High power mode for volatage compensation.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th>Default Value</th> </tr> <tr> <th>HP[3:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	HP[3:0]	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h			
Status	Default Value													
	HP[3:0]													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart														

9.1.68. FRMSEL: Frame Freq. in Temperature range (F0H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	0	0	(F0H)
1st parameter	1	1	0	-	-	-	DIVA	FA3	FA2	FA1	FA0	Range A
2nd parameter	1	1	0	-	-	-	DIVB	FB3	FB2	FB1	FB0	Range B
3rd parameter	1	1	0	-	-	-	DIVC	FC3	FC2	FC1	FC0	Range C
4th parameter	1	1	0	-	-	-	DIVD	FD3	FD2	FD1	FD0	Range D

Description	<p>Select Frame Freq. in normal display mode.</p> <p>1st parameter : Frame freq. value set in temperature range 30(-30) to TA</p> <p>2nd parameter : Frame freq. value set in temperature P range TA to TB</p> <p>3rd parameter : Frame freq. value set in temperature range TB to TC</p> <p>4th parameter : Frame freq. value set in temperature range TC to 145(90)</p> <p>For command setting to frame rate value look-up-table, please see the following table:</p>																																								
	<table border="1"> <thead> <tr> <th>DIVx</th> <th>Fx[3:0]</th> <th>Frame Rate (Hz)</th> </tr> </thead> <tbody> <tr> <td rowspan="14">1</td> <td>0</td> <td>75</td> </tr> <tr> <td>1</td> <td>76</td> </tr> <tr> <td>2</td> <td>77</td> </tr> <tr> <td>3</td> <td>80</td> </tr> <tr> <td>4</td> <td>84</td> </tr> <tr> <td>5</td> <td>88</td> </tr> <tr> <td>6</td> <td>92</td> </tr> <tr> <td>7</td> <td>97</td> </tr> <tr> <td>8</td> <td>102</td> </tr> <tr> <td>9</td> <td>108</td> </tr> <tr> <td>A</td> <td>115</td> </tr> <tr> <td>B</td> <td>123</td> </tr> <tr> <td>C</td> <td>133</td> </tr> <tr> <td>D</td> <td>144</td> </tr> <tr> <td>E</td> <td>155</td> </tr> <tr> <td>F</td> <td>170</td> </tr> <tr> <td>0</td> <td>0~F</td> <td>(Frame Rate) / 2</td> </tr> </tbody> </table>			DIVx	Fx[3:0]	Frame Rate (Hz)	1	0	75	1	76	2	77	3	80	4	84	5	88	6	92	7	97	8	102	9	108	A	115	B	123	C	133	D	144	E	155	F	170	0	0~F
DIVx	Fx[3:0]	Frame Rate (Hz)																																							
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	5	88																																							
	6	92																																							
	7	97																																							
	8	102																																							
	9	108																																							
	A	115																																							
	B	123																																							
	C	133																																							
	D	144																																							
E	155																																								
F	170																																								
0	0~F	(Frame Rate) / 2																																							
Restriction																																									

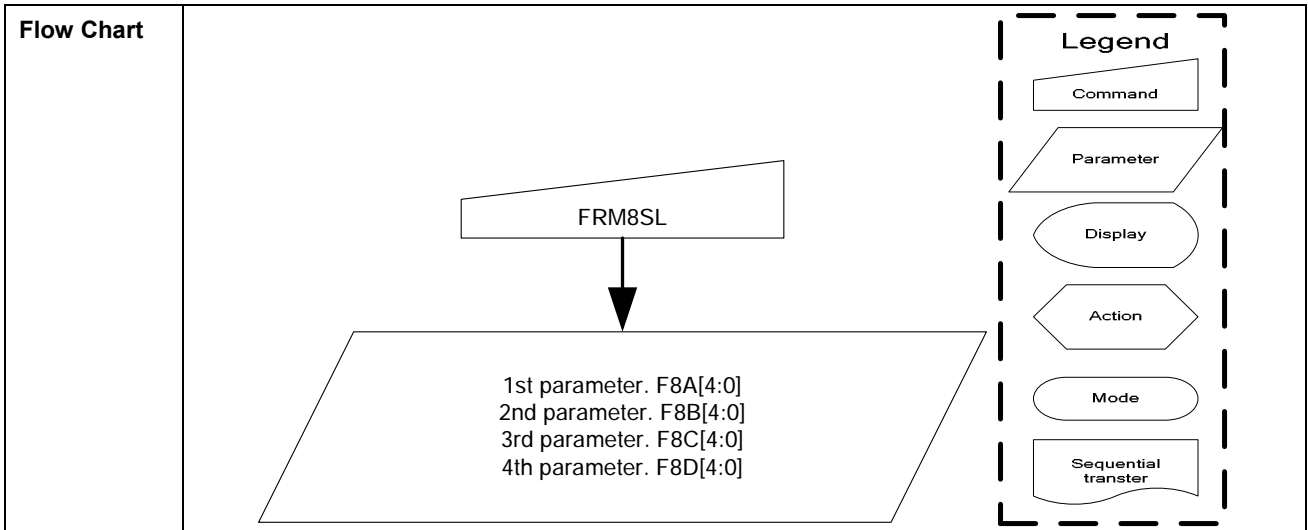
ST7637

Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes												
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Status	Default Value																								
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S/W Reset	06h	0Bh	0Dh	12h																					
H/W Reset	06h	0Bh	0Dh	12h																					
Flow Chart	<p>The flow chart shows a trapezoidal box labeled 'FRMSL' with a downward arrow pointing to a parallelogram box containing the following text:</p> <p>1st parameter. FA[4:0] 2nd parameter. FB[4:0] 3rd parameter. FC[4:0] 4th parameter. FD[4:0]</p> <p>To the right of the flow chart is a legend box with a dashed border, containing the following items:</p> <ul style="list-style-type: none"> Command: Represented by a trapezoid. Parameter: Represented by a parallelogram. Display: Represented by an oval. Action: Represented by a hexagon. Mode: Represented by a rounded rectangle. Sequential transfer: Represented by a rectangle with a wavy bottom edge. 																								

9.1.69. FRM8SEL: Frame Freq. in Temperature range (idle-8 color) (F1H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	0	1	(F1h)
1st parameter	1	1	0	-	-	-	F8A4	F8A3	F8A2	F8A1	F8A0	Range A
2nd parameter	1	1	0	-	-	-	F8B4	F8B3	F8B2	F8B1	F8B0	Range B
3rd parameter	1	1	0	-	-	-	F8C4	F8C3	F8C2	F8C1	F8C0	Range C
4th parameter	1	1	0	-	-	-	F8D4	F8D3	F8D2	F8D1	F8D0	Range D

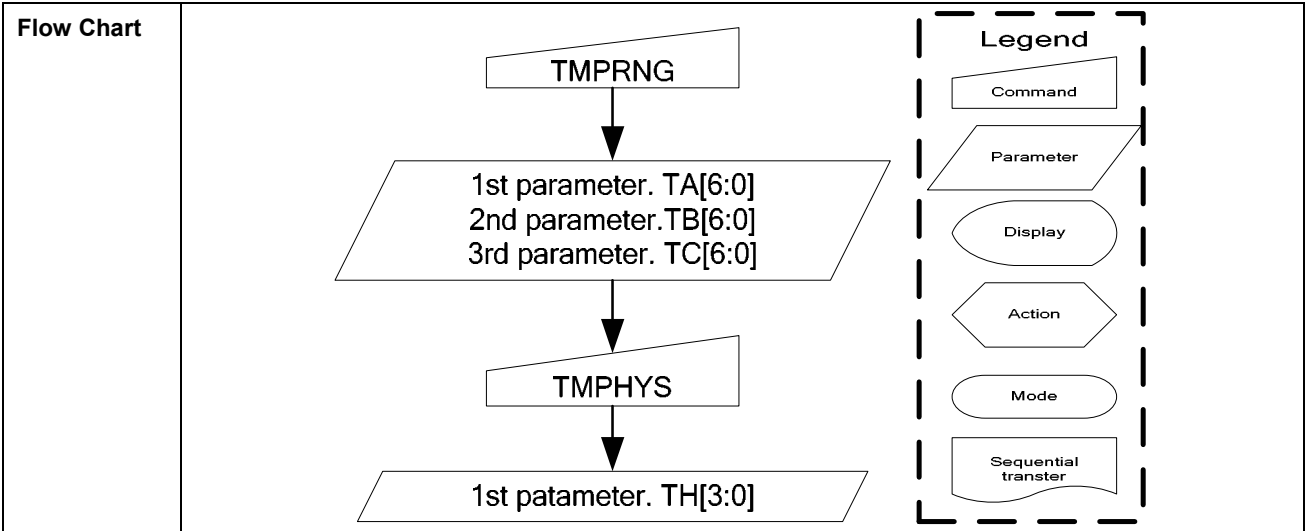
Description	<p>Select Frame Freq. in normal display mode.(idle;8 color mode)</p> <p>1st parameter : Frame freq. value set in TEMP range 30(-30) to TA</p> <p>2nd parameter : Frame freq. value set in TEMP range TA to TB</p> <p>3rd parameter : Frame freq. value set in TEMP range TB to TC</p> <p>4th parameter : Frame freq. value set in TEMP range TC to 145(90)</p>																											
Restriction																												
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Status	Default Value																											
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S/W Reset	06h	0Bh	0Dh	12h																								
H/W Reset	06h	0Bh	0Dh	12h																								



9.1.70. Tmprng: Temp. range set for Frame Freq. Adj. (F2H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	1	0	(F2h)
1st parameter	1	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	Range A
2nd parameter	1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	Range B
3rd parameter	1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	Range C

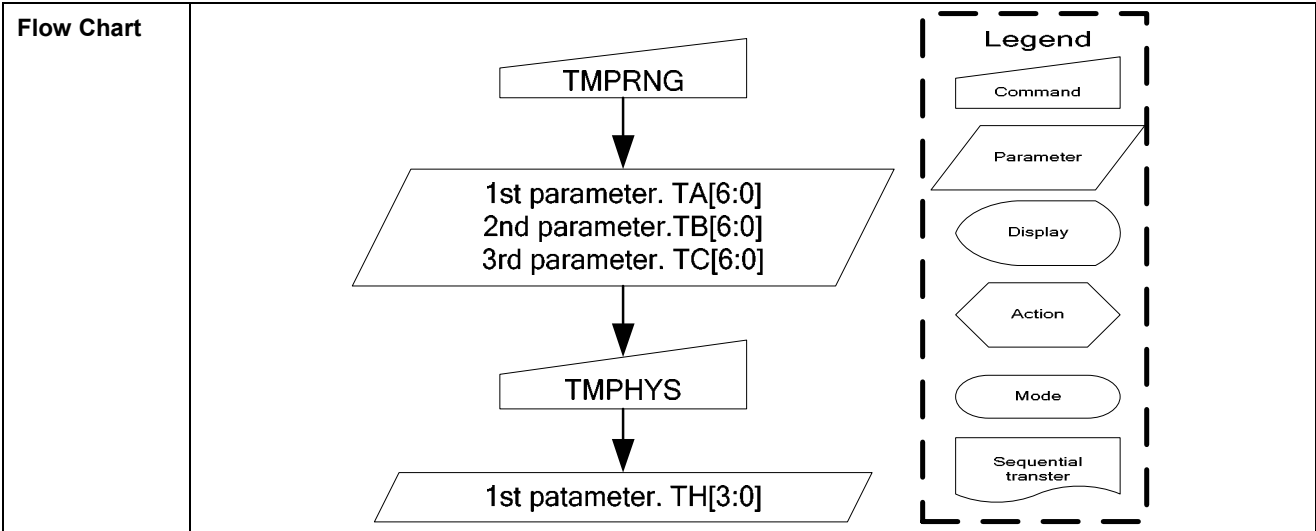
Description	Temp. range set for automatic frame freq. adj. operation according the current temp. value. 1 st parameter: Temp. range A value set 2 nd parameter: Temp. range B value set 3 rd parameter: Temp. range C value set TA/TB/TC Temperature() + 40 = TA/TB/TC[6 :0] Example: If TA wants to be set at 24 , TA[6:0]=24+40=64(40h),																					
Restriction	-40 TA TA+TH TB TB+TH TC 87																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
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Sleep In	Yes																					
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>TA[6:0]</th> <th>TB[6:0]</th> <th>TC[6:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>1Eh</td> <td>28h</td> <td>32h</td> </tr> <tr> <td>S/W Reset</td> <td>1Eh</td> <td>28h</td> <td>32h</td> </tr> <tr> <td>H/W Reset</td> <td>1Eh</td> <td>28h</td> <td>32h</td> </tr> </tbody> </table>			Status	Default Value			TA[6:0]	TB[6:0]	TC[6:0]	Power On Sequence	1Eh	28h	32h	S/W Reset	1Eh	28h	32h	H/W Reset	1Eh	28h	32h
Status	Default Value																					
	TA[6:0]	TB[6:0]	TC[6:0]																			
Power On Sequence	1Eh	28h	32h																			
S/W Reset	1Eh	28h	32h																			
H/W Reset	1Eh	28h	32h																			



9.1.71. TMPHYS: Temp. Hysteresis Set for Frame Freq. Adj. (F3H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	1	1	(F3h)
1 st parameter	1	1	0	-	-	-	-	TH3	TH2	TH1	TH0	

Description	<p>Temp. hysteresis range set for frame freq. adj.</p> <p>Parameter TH[3:0] is used to set Temp. hysteresis range.</p> <p>The relationship between temp. state and temp. range value is shown below.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>TEMP Range Value</th> <th>TEMP Rising State</th> <th>TEMP Falling State</th> </tr> </thead> <tbody> <tr> <td>Freq. changing point A</td> <td>TA[6:0]+TH[3:0]</td> <td>TA[6:0]</td> </tr> <tr> <td>Freq. changing point B</td> <td>TB[6:0]+TH[3:0]</td> <td>TB[6:0]</td> </tr> <tr> <td>Freq. changing point C</td> <td>TC[6:0]+TH[3:0]</td> <td>TC[6:0]</td> </tr> </tbody> </table> <p>TH Temperature() – 1 = TH[3:0]</p> <p>Example: If TH wants to set 5 , TH[3:0]=5-1=4.</p>	TEMP Range Value	TEMP Rising State	TEMP Falling State	Freq. changing point A	TA[6:0]+TH[3:0]	TA[6:0]	Freq. changing point B	TB[6:0]+TH[3:0]	TB[6:0]	Freq. changing point C	TC[6:0]+TH[3:0]	TC[6:0]
TEMP Range Value	TEMP Rising State	TEMP Falling State											
Freq. changing point A	TA[6:0]+TH[3:0]	TA[6:0]											
Freq. changing point B	TB[6:0]+TH[3:0]	TB[6:0]											
Freq. changing point C	TC[6:0]+TH[3:0]	TC[6:0]											
Restriction	Temp. hysteresis value should be smaller than the gap of temp. range.												
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value(TH[3:0])												
Power On Sequence	04h												
S/W Reset	04h												
H/W Reset	04h												



9.1.72. TEMPSEL: Temperature Gradient Compensation Coefficient Set (F4H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEMPSEL	0	1	0	1	1	1	1	0	1	0	0	(F4h)
1 st parameter	1	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00	MT1x: (-24 °C to -32 °C) MT0x: (-32 °C to -40 °C)
2 nd parameter	1	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	MT3x: (-8 °C to -16 °C) MT2x: (-16 °C to -24 °C)
3 rd parameter	1	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	MT5x: (8 °C to 0 °C) MT4x: (0 °C to -8 °C)
4 th parameter	1	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	MT7x: (24 °C to 16 °C) MT6x: (16 °C to 8 °C)
5 th parameter	1	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	MT9x: (40 °C to 32 °C) MT8x: (32 °C to 24 °C)
6 th parameter	1	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	MTBx: (56 °C to 48 °C) MTAx: (48 °C to 40 °C)
7 th parameter	1	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	MTDx: (72 °C to 64 °C) MTCx: (64 °C to 56 °C)
8 th parameter	1	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	MTFx: (87 °C to 80 °C) MTEx: (80 °C to 72 °C)

NOTE: “-“ Don't care

Description	This command defines temperature gradient compensation coefficient. For this command detail description and operation, please see Section 7.11.					
	Parameter n	MT n 3	MT n 2	MT n 1	MT n 0	Voltage / °C
	0	0	0	0	0	+5 mv / °C
	1	0	0	0	1	0 mv / °C
	2	0	0	1	0	-5 mv / °C
	3	0	0	1	1	-10 mv / °C
	:	:	:	:	:	:
	:	:	:	:	:	:
	:	:	:	:	:	:
	12	1	1	0	0	-55 mv / °C
	13	1	1	0	1	-60 mv / °C
	14	1	1	1	0	-65 mv / °C
15	1	1	1	1	-70 mv / °C	
Voltage / °C (+/- 3mv tolerance)						
Restriction						

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (MTn[3:0])
	Power On Sequence	1 st parameter 0xFF
	S/W Reset	2 nd parameter 0x36
	H/W Reset	3 rd parameter 0x04
		4 th parameter 0x00
5 th parameter 0x33		
	6 th parameter 0x42	
	7 th parameter 0xC4	
	8 th parameter 0x59	
Flow Chart	<p>The flow chart illustrates the relationship between the TEMPSEL command and the MTn[3:0] parameter. The TEMPSEL command is represented by a trapezoid, and the MTn[3:0] parameter is represented by a parallelogram. An arrow points from the TEMPSEL command to the MTn[3:0] parameter. A legend on the right side of the chart defines the symbols used: Command (trapezoid), Parameter (parallelogram), Display (oval), Action (hexagon), Mode (rounded rectangle), and Sequential transfer (wavy rectangle).</p>	

9.1.73. THYS : Temperature detection threshold(F7H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
THYS	0	1	0	1	1	1	1	0	1	1	1	(F7h)
Parameter	1	1	0	THYS7	THYS6	THYS5	THYS4	THYS3	THYS2	THYS1	THYS0	-

NOTE: “-“ Don't care

Description	Temperature detection threshold setting.	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value D[7:0]
	Power On Sequence	06h
	S/W Reset	06h
	H/W Reset	06h
Flow Chart	<p>The flow chart illustrates the relationship between the THYS command and its parameter D[7:0]. The command 'THYS' is shown in a trapezoidal shape, with an arrow pointing down to a parallelogram-shaped parameter 'D[7:0]'. To the right, a dashed box labeled 'Legend' defines the symbols used: a trapezoid for 'Command', a parallelogram for 'Parameter', an oval for 'Display', a hexagon for 'Action', a rounded rectangle for 'Mode', and a wavy rectangle for 'Sequential transfer'.</p>	

9.1.74. Frame Set: Frame PWM Set (F9H)

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Frame1 Set	0	1	0	1	1	1	1	1	0	0	1	(F9h)
1 st parameter	1	1	0	-	-	-	P14	P13	P12	P11	P10	-
2 nd parameter	1	1	0	-	-	-	P24	P23	P22	P21	P20	-
:	:	:	:	:	:	:	:	:	:	:	:	-
15 th parameter	1	1	0	-	-	-	P154	P153	P152	P151	P150	-
16 th parameter	1	1	0	-	-	-	P164	P163	P162	P161	P160	-

NOTE: "-“ Don't care

Description	This command is used to set frame PWM.	
Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	--
	S/W Reset	--
	H/W Reset	--
Flow Chart	<pre> graph TD A[Frame 1 Set] --> B[/1st ~ 16th parameters/] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Trapezoid Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Rounded rectangle Sequential transfer: Wavy rectangle 	

NOTE:

The default value of RGB level set

RGB level0	00
RGB level1	01
RGB level2	02
RGB level3	04
RGB level4	06
RGB level5	07
RGB level6	09
RGB level7	0A
RGB level8	0B
RGB level9	0C
RGB level10	0D
RGB level11	0F
RGB level12	11
RGB level13	12
RGB level14	17
RGB level15	1A

All the modulation range of each level for each frame is from 00'H to 1F'H.

10. SPECIFICATIONS

10.1 ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Item	Symbol	Value	Unit
Supply voltage (1)	VDD,VDD1	- 0.3 ~ + 3.0	V
Supply voltage (1)	VDD2,VDD3,VDD4,VDD5	- 0.3 ~ + 4.2	V
Supply voltage (2)	V _{LCD} (V _O -V _{SS})	- 0.3 ~ + 18.0	V
Supply voltage (3)	V _{MAX} (V _O - X _{V0})	- 0.3 ~ + 18.0	V
Input voltage range	V _{IN}	- 0.3 ~ V _{DD} + 0.5	V
Output voltage range	V _O	- 0.3 ~ V _{DD} + 0.5	V
Operating temperature range	T _{OPR}	- 30 ~ + 85	°C
Storage temperature range	T _{STG}	- 40 ~ + 125	°C

NOTE:

(1). Voltages are all based on V_{SS} = 0V.

(2). Voltage relationship: V_O. V_g. V_m. V_{SS}. X_{V0} must always be satisfied.

(3). For External Supply

10.2 DC CHARACTERISTICS

10.2.1. Basic Characteristics

(VSS=0V , Ta = -30 to 85°C)

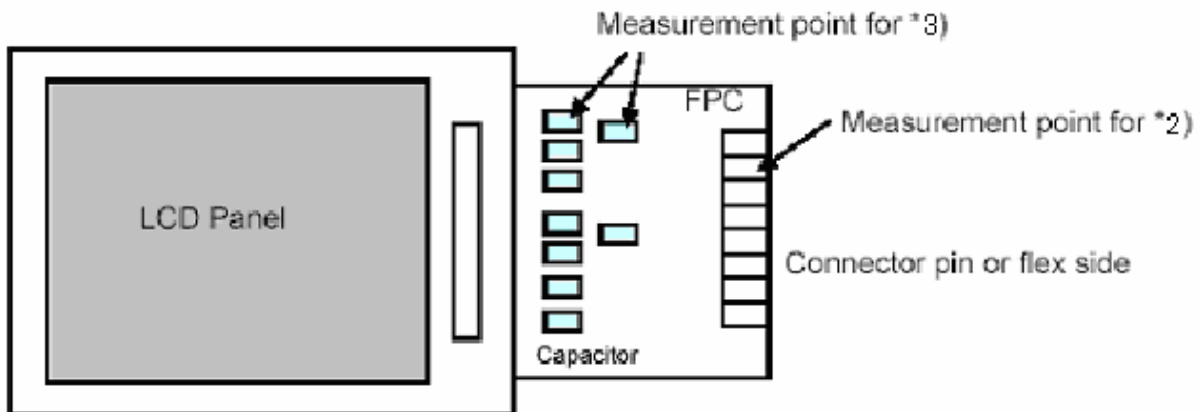
Parameter	Symbol	Conditions	Related Pins	MIN	TYP	MAX	Unit
Logic Operating voltage	VDDI	-	*2)VDD,VDD1	1.65	1.8	3.0	V
Analog Operating voltage	VDDA	-	*2)VDD2,3,4,5	2.4	2.75	3.3	
Driving voltage input	VLCD	V0 – VSS	*3)V0, VSS	-	-	18.0	
	XVLCD	VSS – XV0	*3)VSS, XV0	-	-	18.0	
High level input voltage	VIH		*1) *2)	0.7VDD	-	VDD	
Low level input voltage	VIL	-	*1) *2)	VSS	-	0.3VDD	
High level output voltage	VOH	IOH = -1.0mA	*2) SI, TE	0.8VDD	-	VDD	
Low level output voltage	VOL	IOL = +1.0mA		VSS	-	0.2VDD	
Input leakage current	IIL	VIN = VDD or Vss	*1) *2)	-1.0	-	+1.0	μA
Driver on resistance (SEG)	RONSEG	Vg = 5.0V	S0 to S395	-	0.5	-	KΩ
Driver on resistance (COM)	RONCOM	V0 = 10.0V	C0 to C131	-	0.5	-	
External oscillator frequency	fOSC	fFR=77Hz	OSC	-	630	-	kHz
Reference voltage	VREF	No load	-	1.75	1.8	1.85	V
Voltage follower output voltage	Vm	Ta = 25°C	-	0.7	Vg/2	VDDA-0.7	V
	Vg		-	1.8	-	VDDAX2	V

NOTE:

*1) Applies to IF1, IF2, IF3, /CS, /RST, /WR, /RD, A0(SCL) and D15-D2, D1 (A0) ,D0(SI) pins

*2) *3) When the measurements are performed with LCD module, Measurement Points are like below.

*4) Vdda cannot be higher than 3V while Vddi<1.7V.



10.2.2. Current Consumption

Operation mode	Image	Memory Data Access Control (MY:MX:MV)	Current consumption			
			Typical		Worst case	
			IDDA (mA)	IDDI (mA)	IDDA (mA)	IDDI (mA)
- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	Note 1	X;X;X	0.45	0.1	0.5	0.15
	Note 2	X;X;X	0.45	0.1	0.5	0.15
	Note 3	X;X;X	0.45	0.1	0.5	0.15
	Note 4	X;X;X	0.5	0.1	0.6	0.15
	Note 5	X;X;X	0.5	0.1	0.6	0.15
	Note 8	X;X;X	0.6	0.1	0.7	0.15
- Normal Mode On - Partial Mode Off - Idle Mode On - Sleep Out Mode	Note 5	X;X;X	0.4	0.1	0.5	0.1
- Normal Mode Off - Partial Mode On (40 lines) - Idle Mode Off - Sleep Out Mode	Grey Levels	X;X;X	0.35	0.1	0.40	0.15
- Normal Mode Off - Partial Mode On (40 lines) - Idle Mode On - Sleep Out Mode	Note 7	X;X;X	0.25	0.1	0.3	0.1
	Note 8	X;X;X	0.35	0.15	0.4	0.15
- Sleep In Mode	N/A	N/A	0.006	0.004	0.015	0.01
- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	65K Colors Note 9 CPU Access @ 15fps	0;0;0	0.45	0.4	0.6	0.45
		0;0;1	0.45	0.4	0.6	0.45
		0;1;0	0.45	0.4	0.6	0.45
		0;1;1	0.45	0.4	0.6	0.45
		1;0;0	0.45	0.4	0.6	0.45
		1;0;1	0.45	0.4	0.6	0.45
		1;1;0	0.45	0.4	0.6	0.45
	65K Colors Note 9 CPU Access @ 25fps	0;0;0	0.45	0.5	0.6	0.55
		0;0;1	0.45	0.5	0.6	0.55
		0;1;0	0.45	0.5	0.6	0.55
		0;1;1	0.45	0.5	0.6	0.55
		1;0;0	0.45	0.5	0.6	0.55
		1;0;1	0.45	0.5	0.6	0.55
		1;1;0	0.45	0.5	0.6	0.55
1;1;1	0.45	0.5	0.6	0.55		

Notes

X: do not care

- 1. All pixels white*
- 2. Checker board one by one*
- 3. Checker board 4 by 4*
- 4. Grey scale from top to bottom*
- 5. 20% White, 80% Black*
- 6. CPU access is inactive.*
- 7. Black & White Checker board 8 by 8.*
- 8. Absolute Worst Case Patterns: Defined by Display Supplier*
- 9. Absolute Worst Case Patterns and Sequences: Defined by Display Supplier*

Typical Case:

TA = 25°C

VDDA = 2.8V

VDDI = 1.8V

Worst Case:

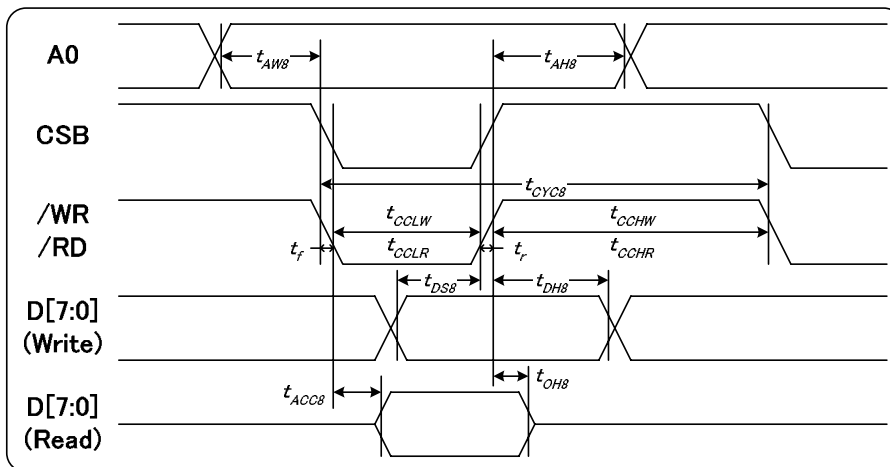
TA = 25°C

VDDA = 2.4V to 3.3V

VDDI = 1.65V to 3.0V

11. TIMING CHARACTERISTICS

11.1 Parallel Interface Characteristics bus (8080-series MCU)



($V_{DD}=2.8V$, $T_a=-30^{\circ}C$ to $85^{\circ}C$, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		15	—	ns
Address setup time		tAW8		15	—	
System cycle time (WRITE)	WR	tCYC8		170	—	
/WR L pulse width (WRITE)		tCCLW		50	—	
/WR H pulse width (WRITE)		tCCHW		100	—	
System cycle time (READ)	RD (ID)	tCYC8		60	—	
/RD L pulse width (READ)		tCCLR	When read ID data	40	—	
/RD H pulse width (READ)		tCCHR		20	—	
System cycle time (READ)	RD (FM)	tCYC8	When read from frame memory	180	—	ns
/RD L pulse width (READ)		tCCLR		55	—	
/RD H pulse width (READ)		tCCHR		90	—	
WRITE data setup time	D0 to D7	tDS8		50	—	
WRITE data hold time		tDH8		10	—	
READ access time (ID)		tACC8 (ID)		—	50	
READ access time (FM)		tACC8 (FM)	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	—	60	

(V_{DD}=1.8V, Ta= -30°C to 85°C, die)

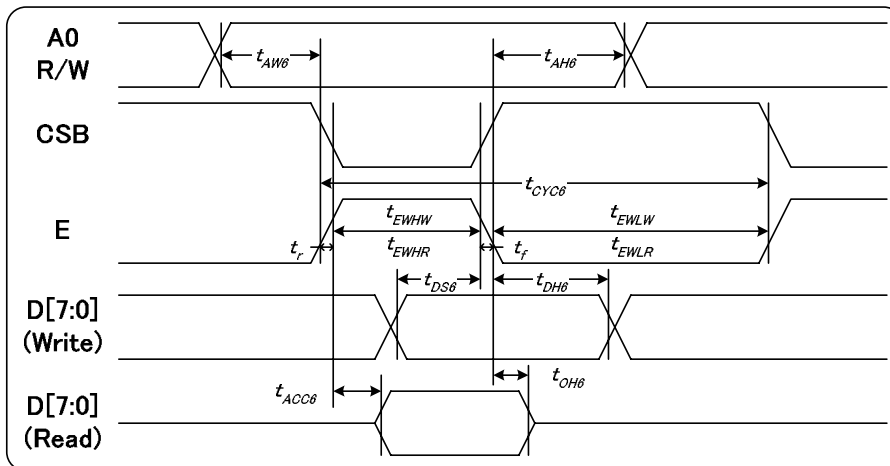
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		15	—	ns
Address setup time		tAW8		15	—	
System cycle time (WRITE)	WR	tCYC8		260	—	ns
/WR L pulse width (WRITE)		tCCLW		60	—	
/WR H pulse width (WRITE)		tCCHW		170	—	
System cycle time (READ)	RD (ID)	tCYC8	When read ID data	110	—	
/RD L pulse width (READ)		tCCLR		70	—	
/RD H pulse width (READ)		tCCHR		25	—	
System cycle time (READ)	RD (FM)	tCYC8	When read from frame memory	450	—	
/RD L pulse width (READ)		tCCLR		100	—	
/RD H pulse width (READ)		tCCHR		220	—	
WRITE data setup time	D0 to D7	tDS8		60	—	
WRITE data hold time		tDH8		10	—	
READ access time (ID)		tACC8 (ID)		—	60	
READ access time (FM)		tACC8 (FM)	CL = 100 pF	—	90	
READ Output disable time		tOH8	CL = 100 pF	—	80	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) (tCYC8 – tCCLW – tCCHW) for (tr + tf) (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between /CS being “L” and WR and RD being at the “L” level.

11.2 Parallel Interface Characteristics bus (6800-series MCU)



(V_{DD}=2.8V, T_a= -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAW8		10	—	
System cycle time (WRITE)	E	tCYC8		130	—	ns
/WR L pulse width (WRITE)		tCCLW		80	—	
/WR H pulse width (WRITE)		tCCHW		45	—	
System cycle time (READ)	RD (ID)	tCYC8		65	—	ns
/RD L pulse width (READ)		tCCLR	When read ID data	15	—	
/RD H pulse width (READ)		tCCHR		35	—	
System cycle time (READ)	RD (FM)	tCYC8		180	—	ns
/RD L pulse width (READ)		tCCLR	When read from frame memory	130	—	
/RD H pulse width (READ)		tCCHR		50	—	
WRITE data setup time	D0 to D7	tDS8		50	—	ns
WRITE data hold time		tDH8		10	—	
READ access time (ID)		tACC8 (ID)		—	70	
READ access time (FM)		tACC8 (FM)	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	—	60	

(V_{DD}=1.8V, Ta= -30°C to 85°C, die)

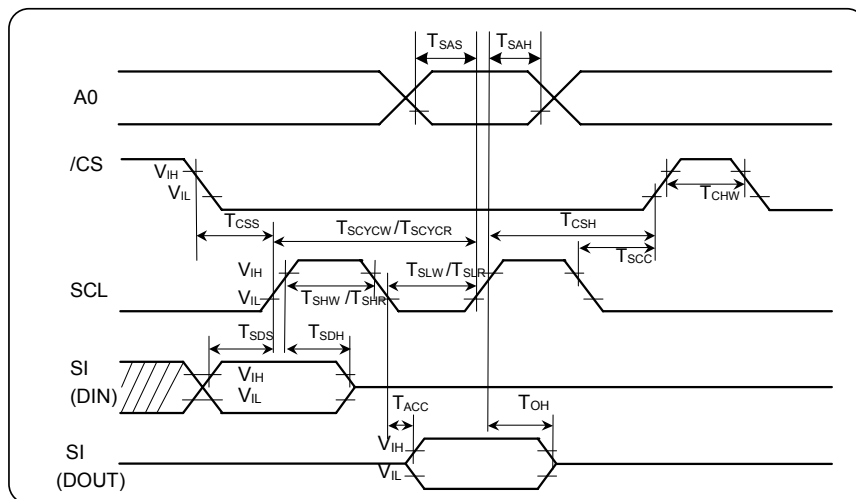
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAW8		10	—	
System cycle time (WRITE)	E	tCYC8		210	—	ns
/WR L pulse width (WRITE)		tCCLW		150	—	
/WR H pulse width (WRITE)		tCCHW		50	—	
System cycle time (READ)	RD (ID)	tCYC8	When read ID data	110	—	
/RD L pulse width (READ)		tCCLR		25	—	
/RD H pulse width (READ)		tCCHR		70	—	
System cycle time (READ)	RD (FM)	tCYC8	When read from frame memory	400	—	
/RD L pulse width (READ)		tCCLR		200	—	
/RD H pulse width (READ)		tCCHR		200	—	
WRITE data setup time	D0 to D7	tDS8		60	—	
WRITE data hold time		tDH8		10	—	
READ access time (ID)		tACC8 (ID)			60	
READ access time (FM)		tACC8 (FM)	CL = 100 pF	—	90	
READ Output disable time		tOH8	CL = 100 pF	—	80	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) (tCYC6 – tEWLW – tEWHW) for (tr + tf) (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between /CS being “L” and E.

11.3 Serial Interface Characteristics (4-pin Serial)



($V_{DD}=2.8V$, $T_a = -30^{\circ}C$ to $85^{\circ}C$, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period (write)	SCL	t_{SCYCW}		40	—	ns
SCL "H" pulse width (write)		t_{SHW}		20	—	
SCL "L" pulse width (write)		t_{SLW}		20	—	
Serial clock period (read)		t_{SCYCR}		40	—	
SCL "H" pulse width (read)		t_{SHR}		20	—	
SCL "L" pulse width (read)		t_{SLR}		20	—	
Address setup time	A0	t_{SAS}		10	—	
Address hold time		t_{SAH}		20	—	
Data setup time	SI	t_{SDS}		10	—	
Data hold time		t_{SDH}		20	—	
CS-SCL time	/CS	t_{CSS}		10	—	
CS-SCL time		t_{CSH}		20	—	

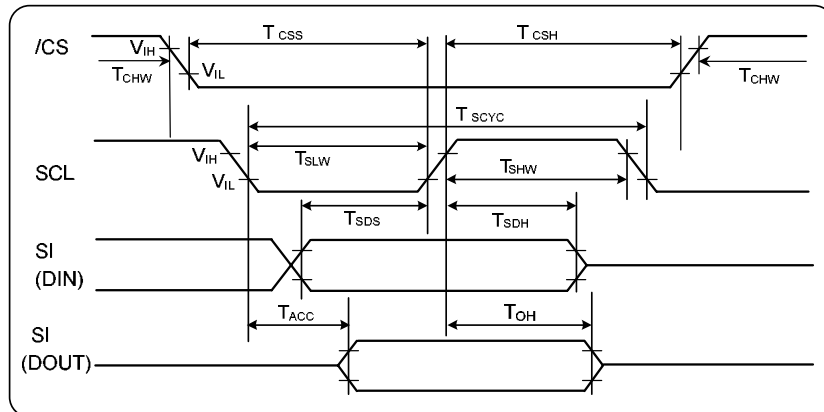
(V_{DD}=1.8V, Ta= -30°C to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period (write)	SCL	tSCYCW		50	—	ns
SCL "H" pulse width (write)		tSHW		25	—	
SCL "L" pulse width (write)		tSLW		25	—	
Serial clock period (read)		tSCYCR		50	—	
SCL "H" pulse width (read)		tSHR		25	—	
SCL "L" pulse width (read)		tSLR		25	—	
Address setup time	A0	tSAS		10	—	
Address hold time		tSAH		25	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		25	—	
CS-SCL time	/CS	tCSS		10	—	
CS-SCL time		tCSH		25	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

11.4 Serial Interface Characteristics (3-pin Serial)



($V_{DD}=2.8V$, $T_a = -30^{\circ}C$ to $85^{\circ}C$, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period (write)	SCL	tSCYC		40	—	ns
SCL "H" pulse width (write)		tSHW		20	—	
SCL "L" pulse width (write)		tSLW		20	—	
Serial clock period (read)		tSCYC		40	—	
SCL "H" pulse width (read)		tSHW		20	—	
SCL "L" pulse width (read)		tSLW		20	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		20	—	
CS-SCL time	/CS	tCSS		10	—	
CS-SCL time		tCSH		20	—	

(V_{DD}=1.8V, Ta= -30°C to 85°C, die)

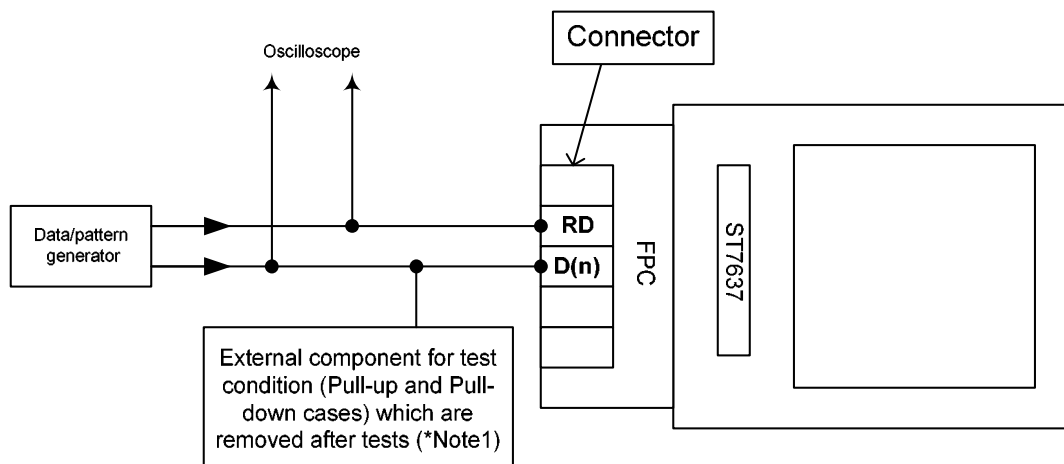
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period (write)	SCL	tSCYC		50	—	ns
SCL "H" pulse width (write)		tSHW		25	—	
SCL "L" pulse width (write)		tSLW		25	—	
Serial clock period (read)		tSCYC		50	—	
SCL "H" pulse width (read)		tSHW		25	—	
SCL "L" pulse width (read)		tSLW		25	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		25	—	
CS-SCL time	/CS	tCSS		10	—	
CS-SCL time		tCSH		25	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

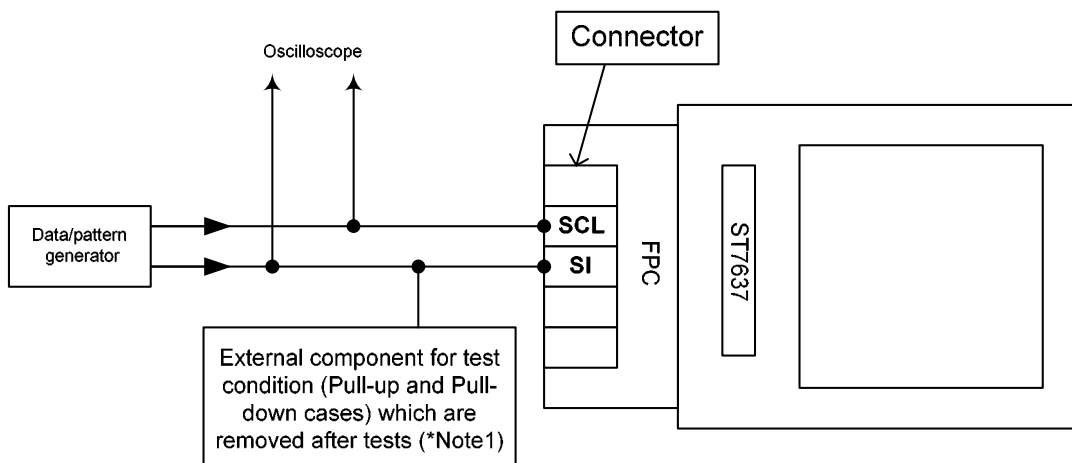
*2 All timing is specified using 20% and 80% of VDD as the standard.

11.5 Output access/disable timing measurement method

Parallel interface (8080-series)



Serial interface (3-line)

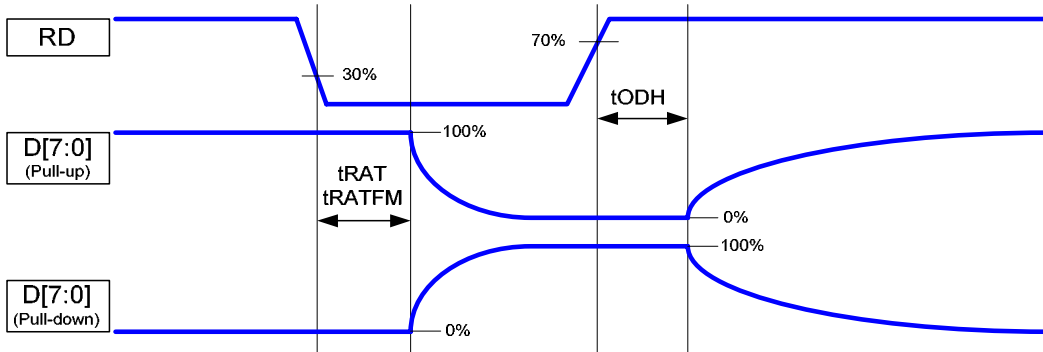


Note:

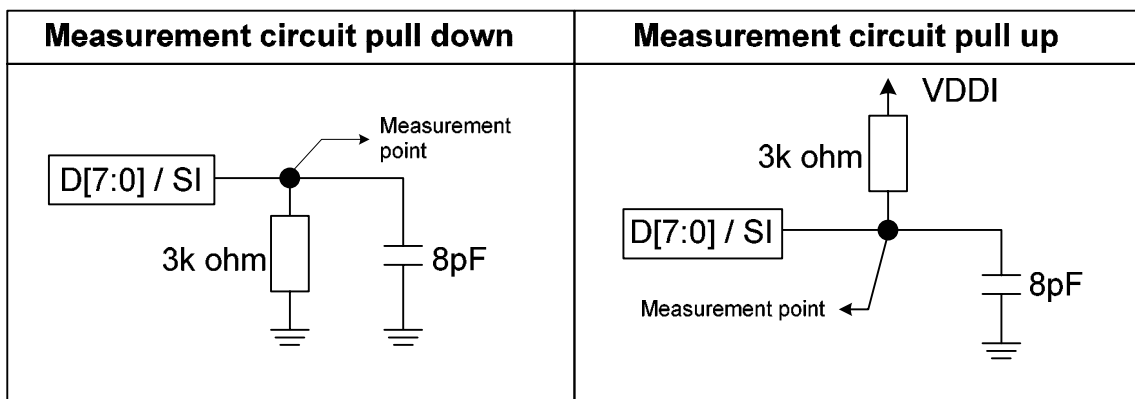
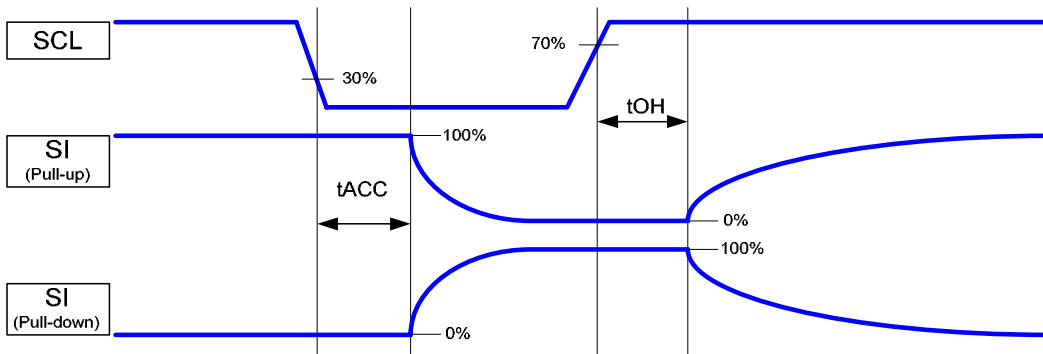
1. pull-up/pull-down resistor: $3K\Omega \pm 5\%$; pull-up/pull-down capacitor: **8 or 30 pF $\pm 10\%$**
2. Capacitances and resistances of the oscilloscope's probe must be included external components in these measurements.

11.5.1.1. Minimum value measurement

Parallel interface (8080-series)

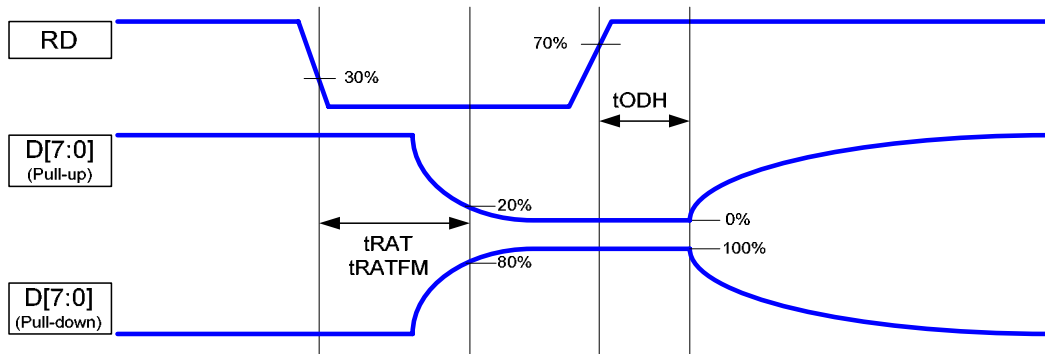


Serial interface (3-line)

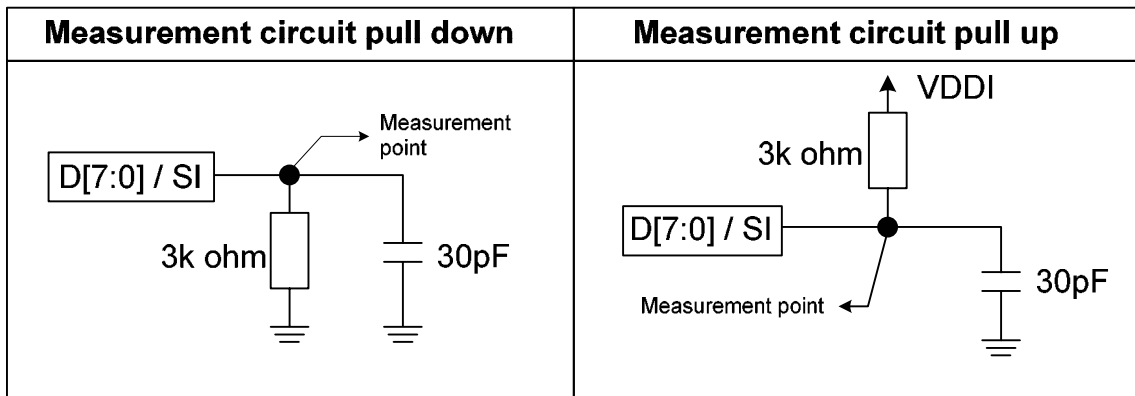
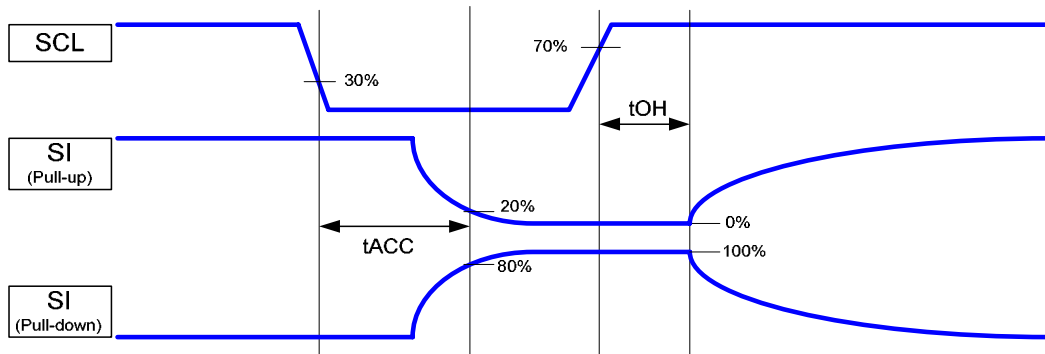


11.5.1.2. Maximum value measurement

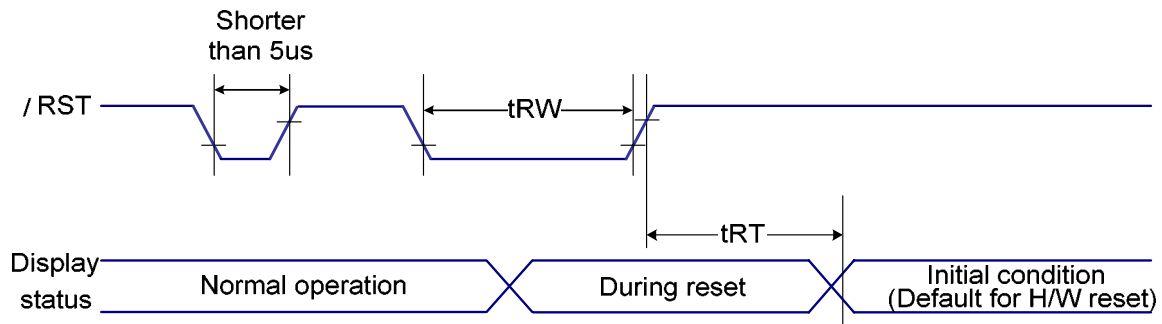
Parallel interface (8080-series)



Serial interface (3-line)



12. RESET TIMING



(VDD=2.8V, Ta = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Reset "L" pulse width	\overline{RST}	t_{RW}		10	—	us
Reset time		t_{RT}		—	5 (*note 5)	ms
				—	120 (*note 6,7)	ms

(VDD=1.8V, Ta = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Reset "L" pulse width	\overline{RST}	t_{RW}		10	—	us
Reset time		t_{RT}		—	5 (*note 5)	ms
				—	120 (*note 6,7)	ms

Notes:

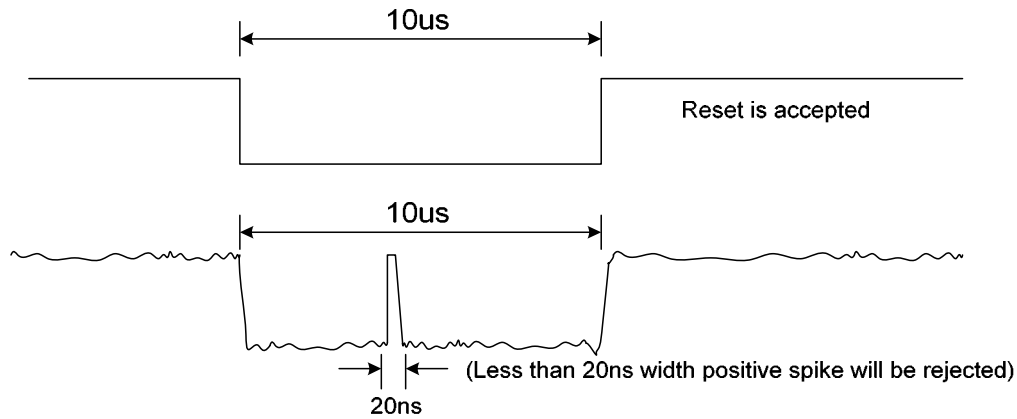
- The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of \overline{RST}
- Spike due to an electrostatic discharge on \overline{RST} line does not cause irregular system reset according to the table below:

RST Pulse	Action
Shorter than 5 μ s	Reset Rejected
Longer than 9 μ s	Reset
Between 5 μ s and 9 μ s	Reset starts

ST7637

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

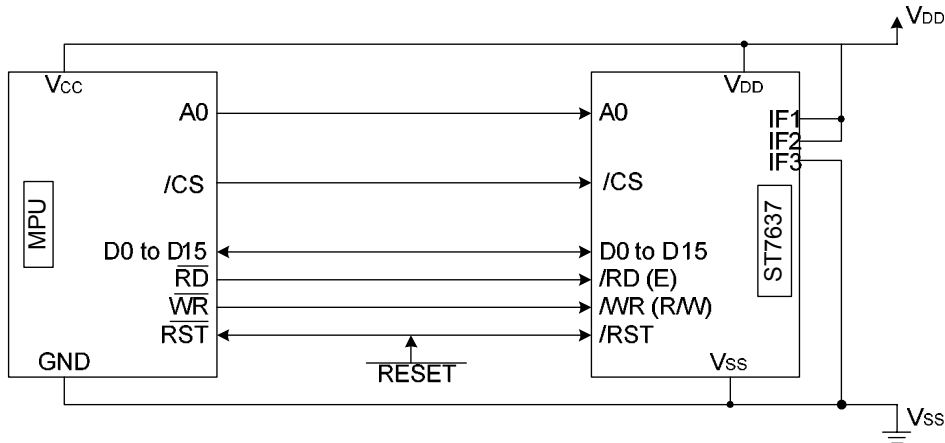
7. It is necessary to wait 5msec after releasing RST before sending commands. Also Sleep Out command cannot be sent for 120msec.

13. THE MPU INTERFACE (REFERENCE EXAMPLES)

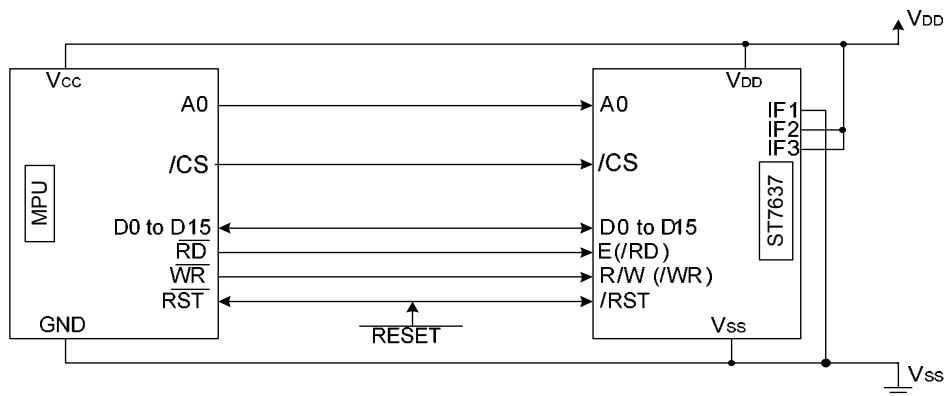
The ST7637 Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7637 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7637 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

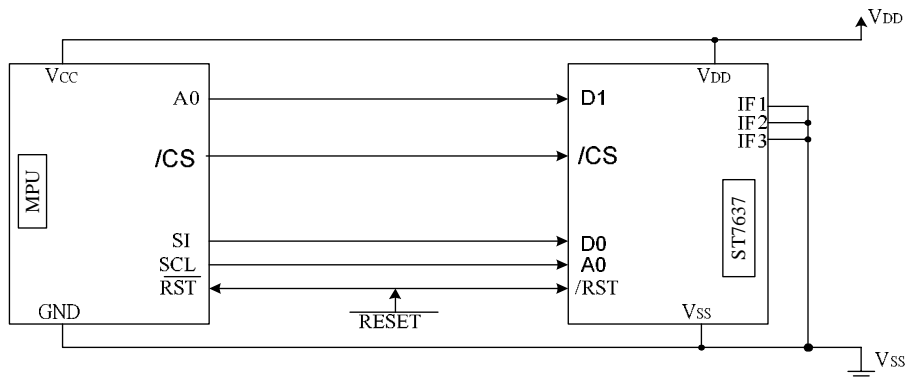
(1) 8080 Series MPUs



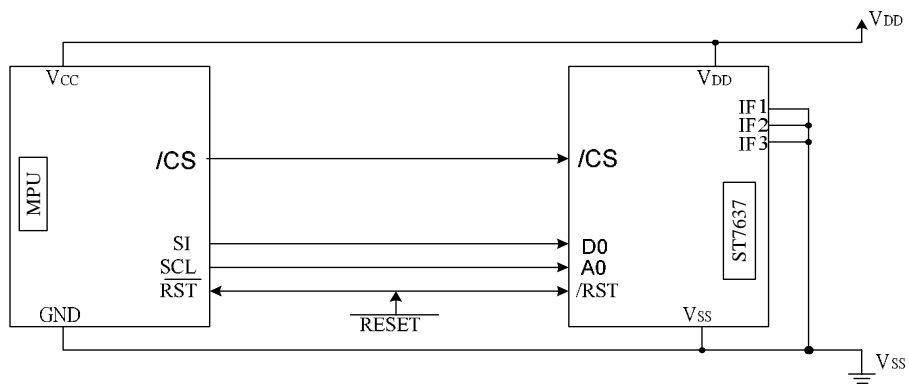
(2) 6800 Series MPUs



(3) Using the Serial Interface (4-line interface)



(4) Using the Serial Interface (3-line interface)

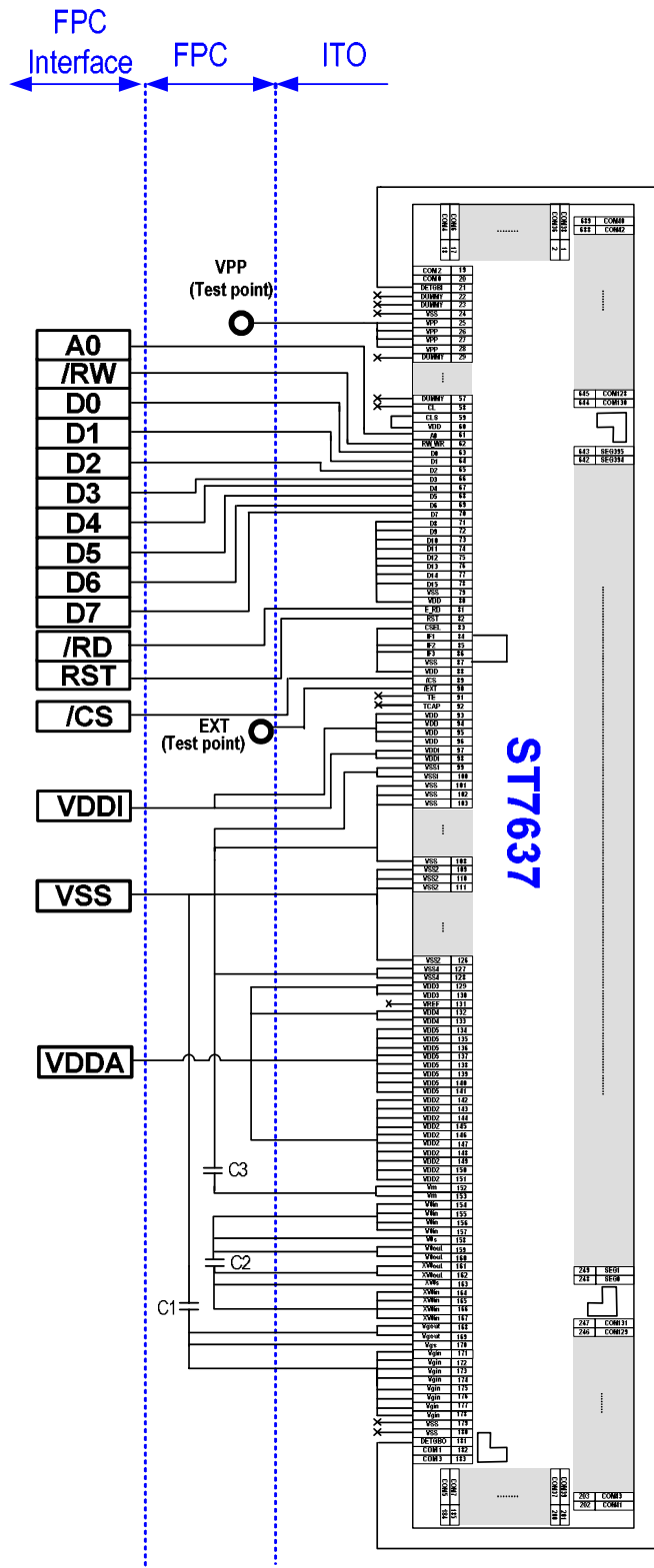


ST7637

A – Application Note

A1a – 80 series 8-bit parallel interlace Mode

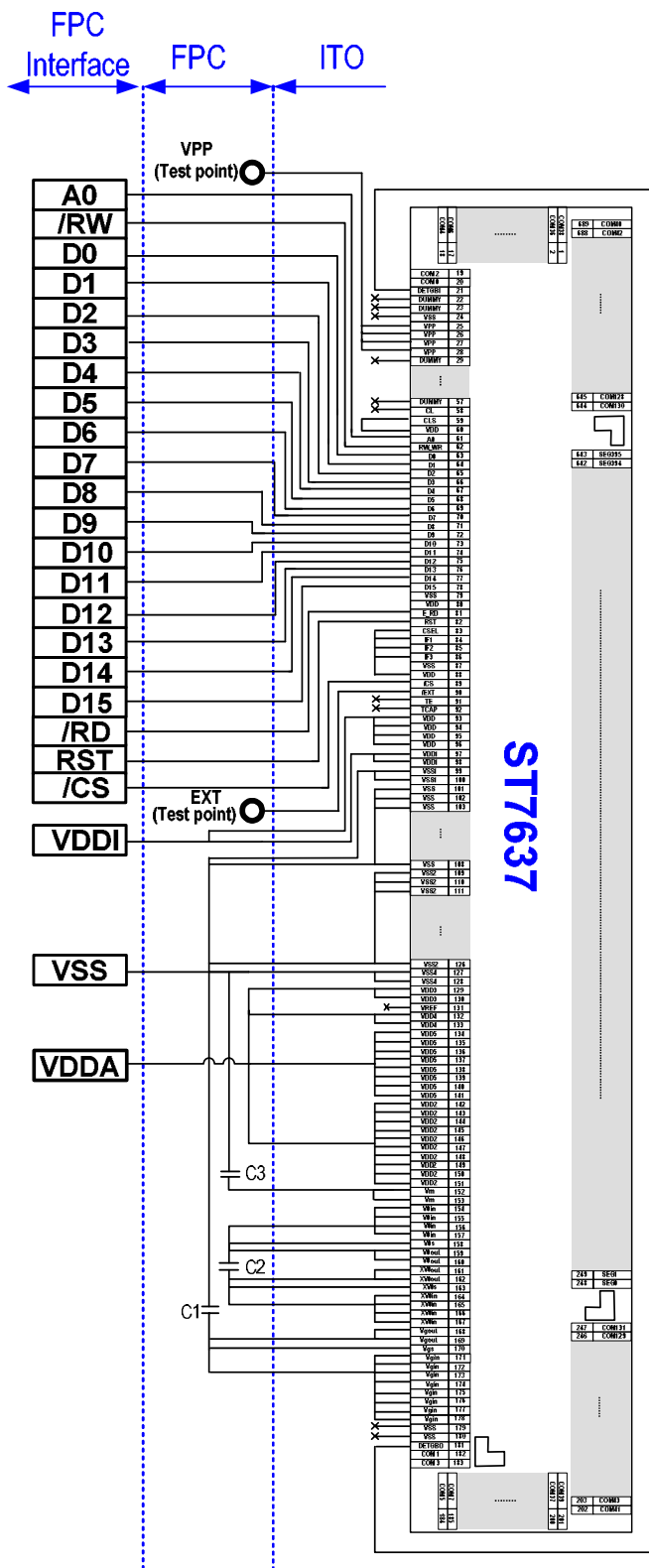
IF[3:1]	HHL
CLS	H (internal OSC)
CSEL	H
C1	1uF/16V
C2	1uF/25V
C3	1uF/16V



ST7637

A1b – 80 series 16-bit parallel interface Mode

IF[3:1]	HHH
CLS	H (internal OSC)
CSEL	H
C1	1uF/16V
C2	1uF/25V
C3	1uF/16V

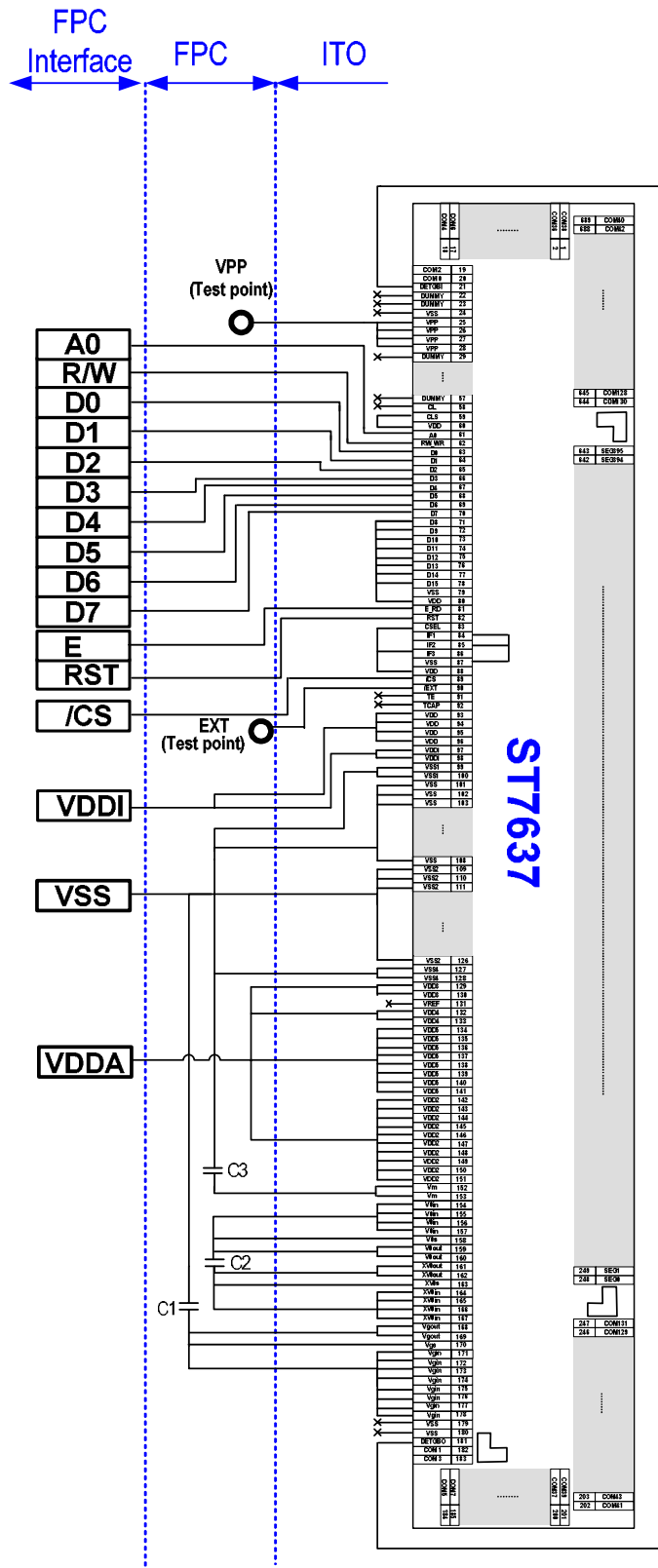


ST7637

ST7637

A1c – 68 series 8-bit parallel interface Mode

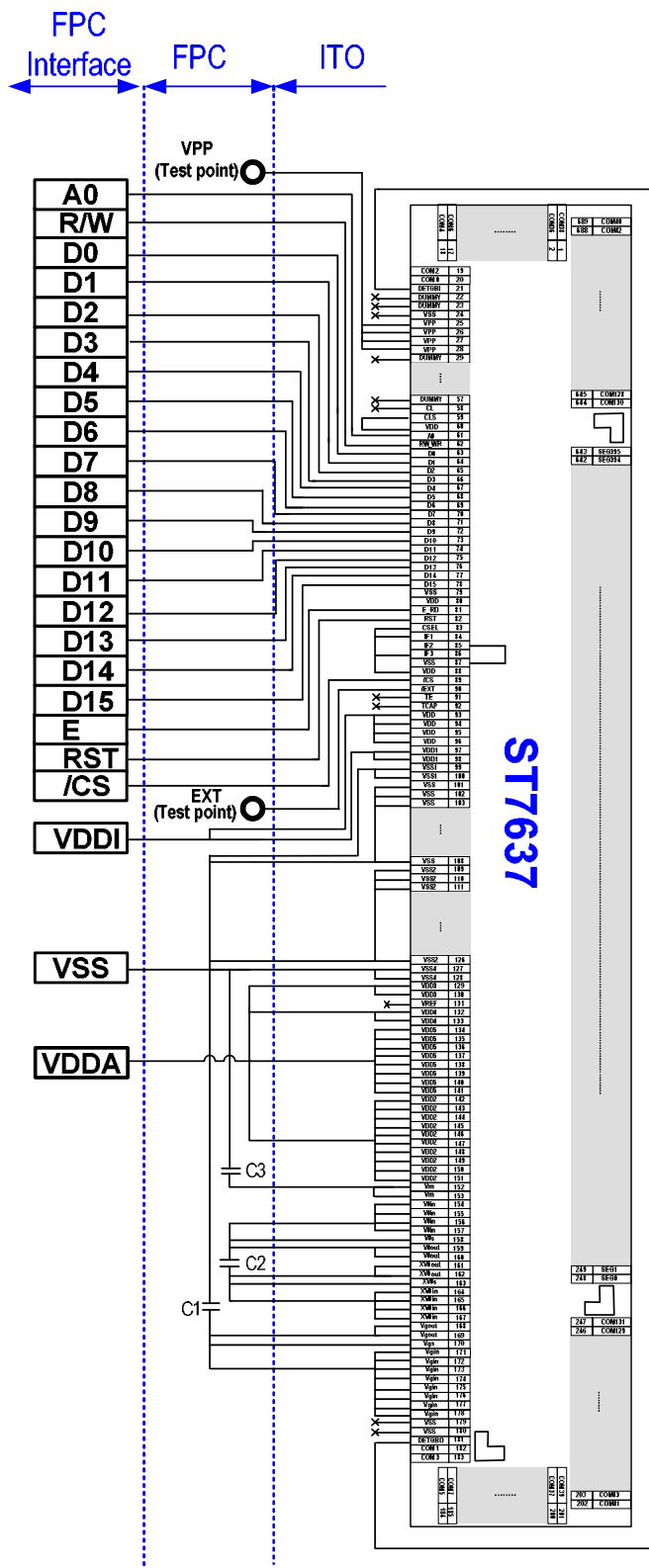
F[3:1]	HLL
CLS	H (internal OSC)
CSEL	H
C1	1uF/16V
C2	1uF/25V
C3	1uF/16V



ST7637

A1d – 68 series 16-bit parallel interlace Mode

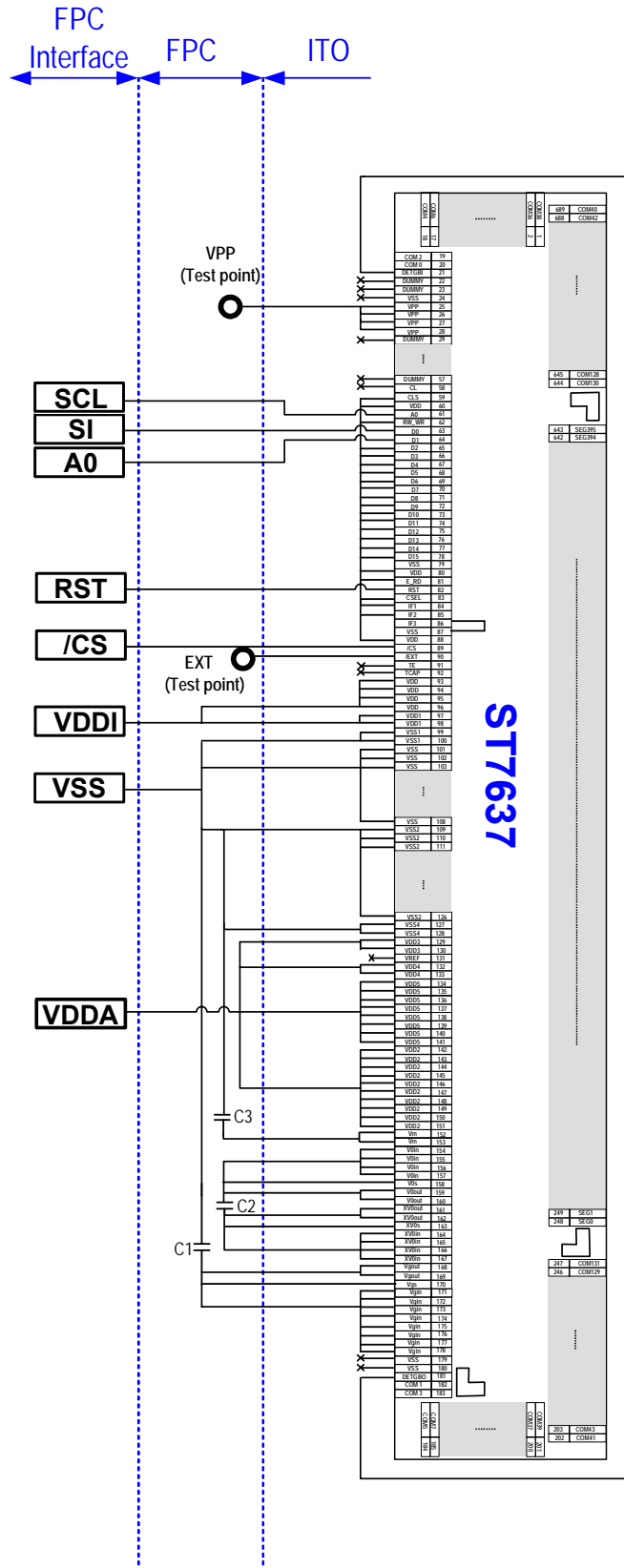
IF[3:1]	HLH
CLS	H (internal OSC)
CSEL	H
C1	1uF/16V
C2	1uF/25V
C3	1uF/16V



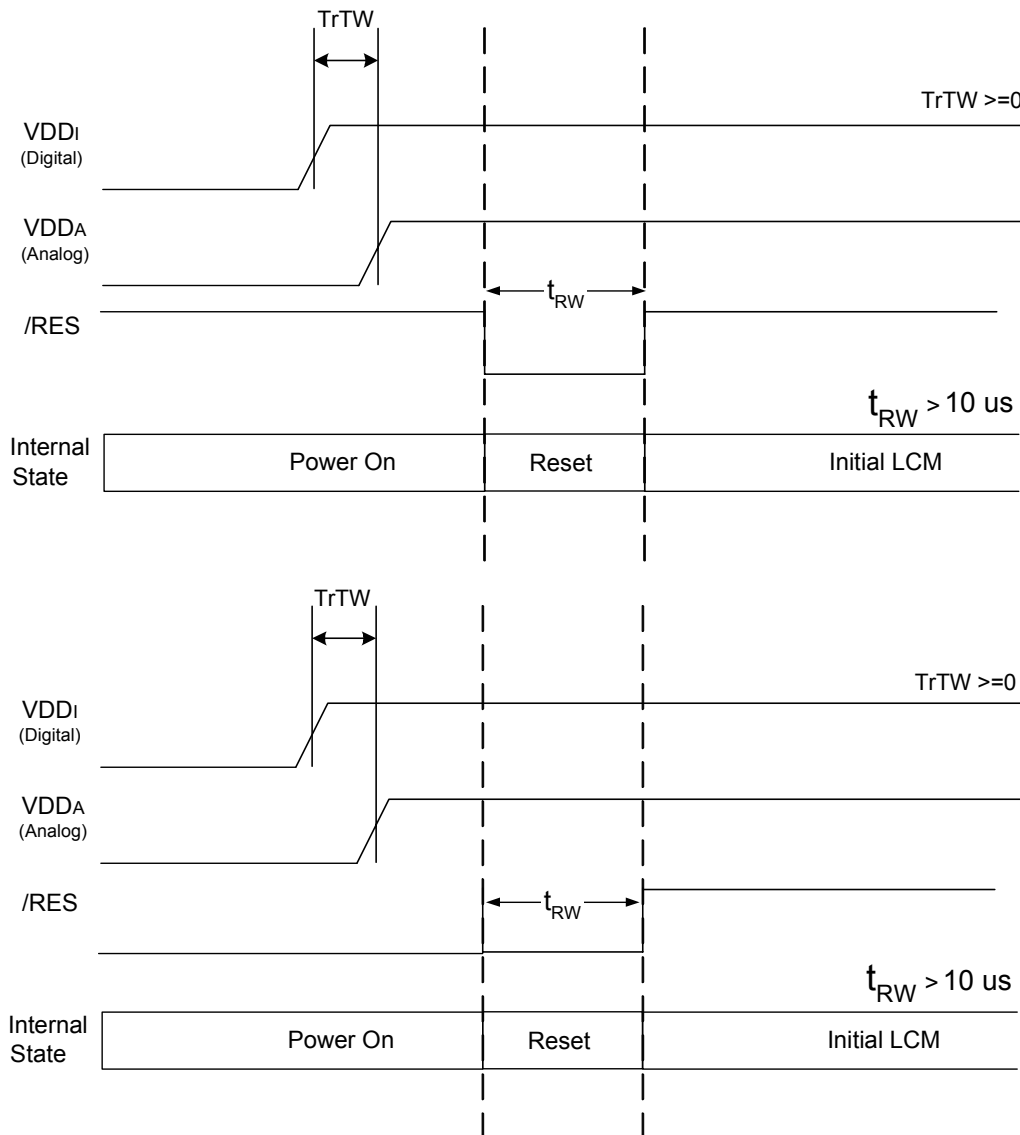
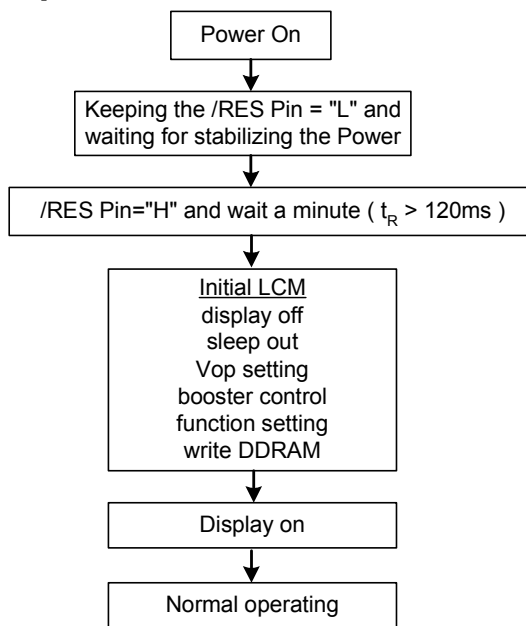
ST7637

A1e – 4-line serial interlace Mode

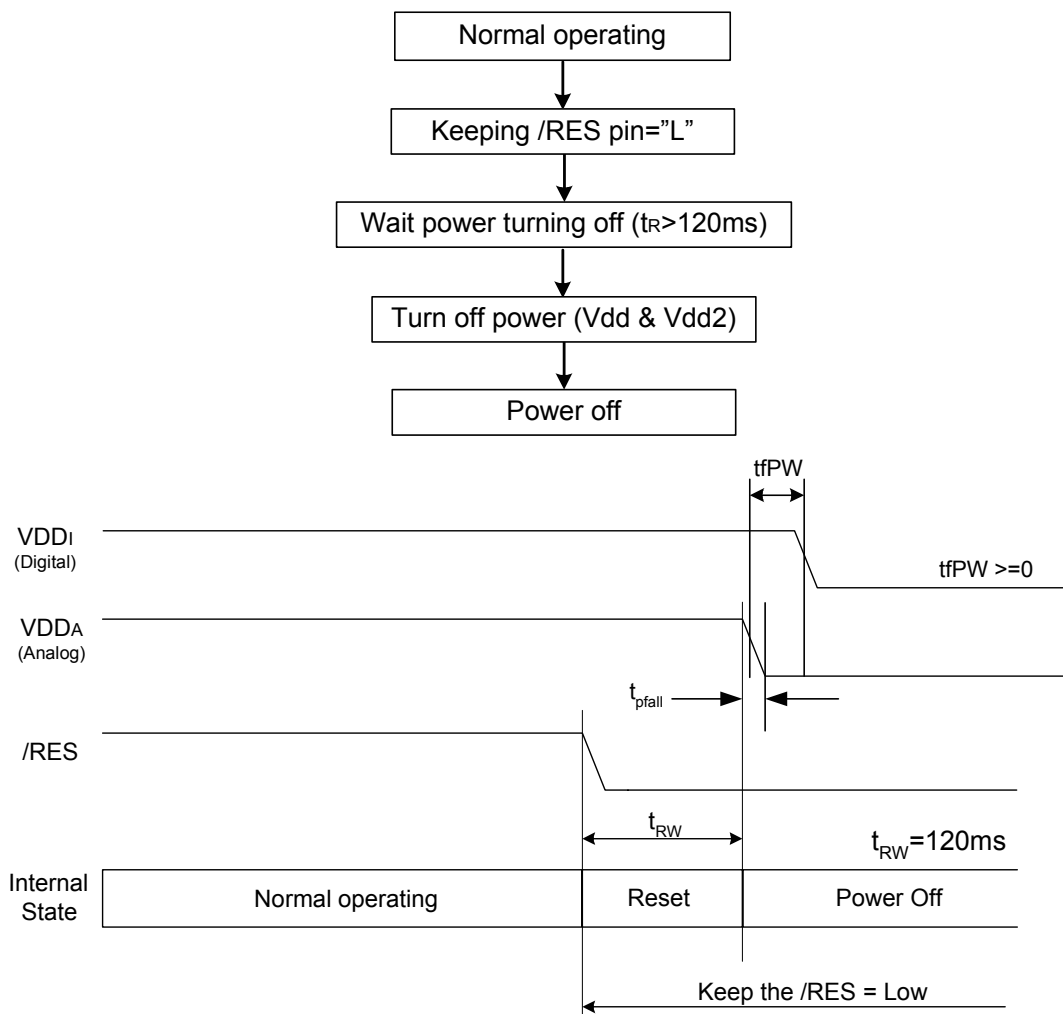
IF[3:1]	LHH
CLS	H (internal OSC)
CSEL	H
C1	1uF/16V
C2	1uF/25V
C3	1uF/16V



A2 – Power on flow and sequence:



◆ A3 – Power off flow and sequence

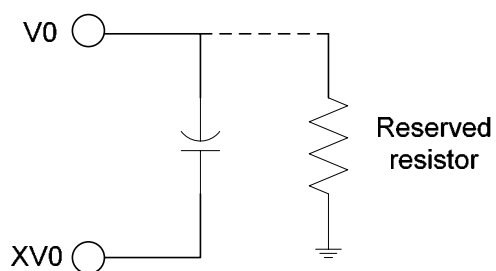


Note:

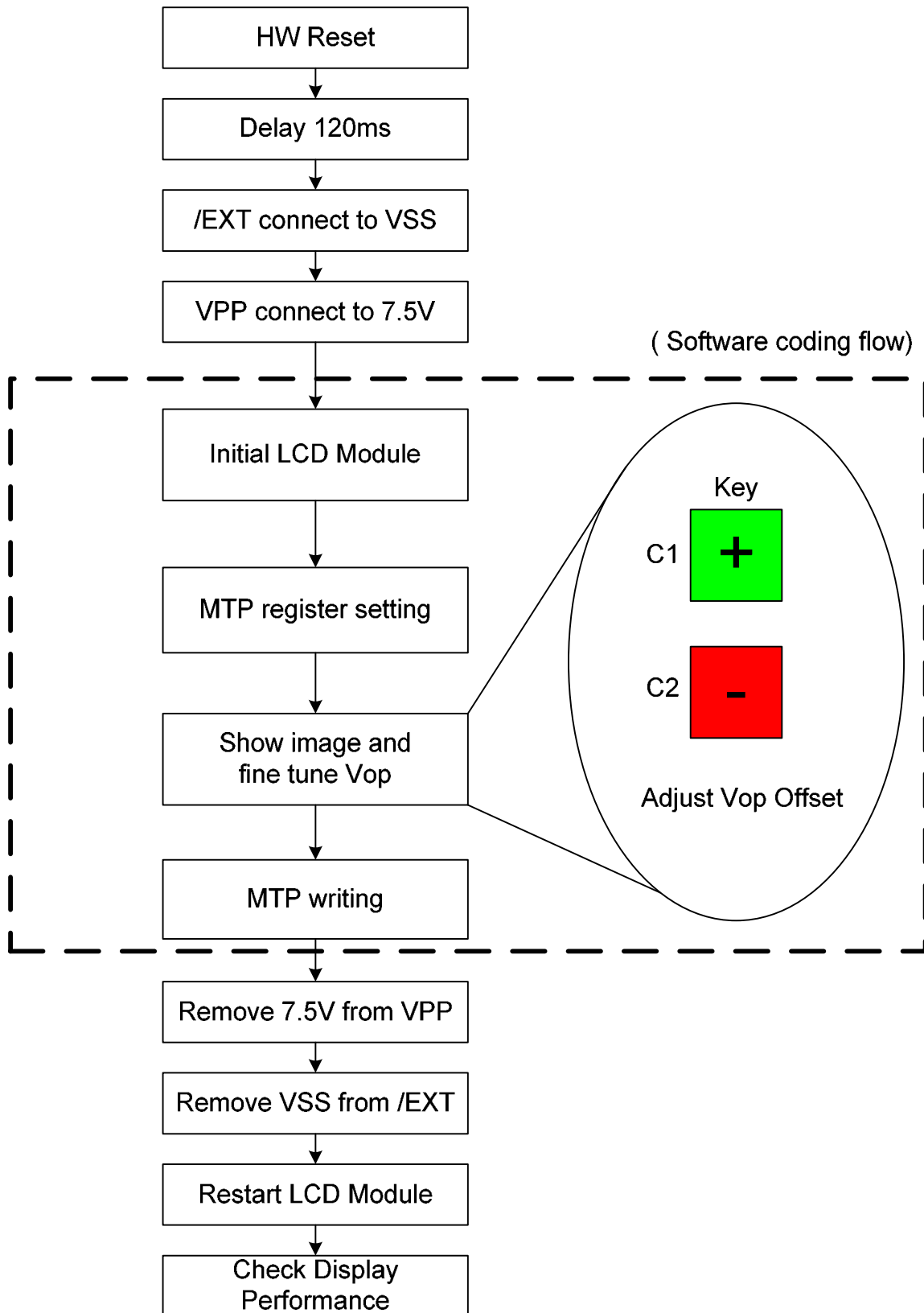
1. When turning VDD_A OFF, the falling time should follow the specification:

$$t_{pFall} \leq 300\text{msec}$$

2. If the power off flow cannot meet this specification, it's recommend to use the resistor shown as blow.



◆ A4 –OTP Burning Flow:



◆ A5 –Software coding flow:

void Initial_LCD_Module(void)			
{			
//-----disable autoread + Manual read once -----			
	Write(COMMAND,0xd7);		// Auto Load Set
	Write(DATA,0x9f);		// Auto Load Disable
	Write(COMMAND,0xE0);		// EE Read/write mode
	Write(DATA,0x00);		// Set read mode
	delayms(10);		// Delay 10ms
	Write(COMMAND,0xE3);		// Read active
	delayms(20);		// Delay 20ms
	Write(COMMAND,0xE1);		// Cancel control
//----- Sleep OUT -----			
	Write(COMMAND, 0x28);		// display off
	Write(COMMAND, 0x11);		// Sleep Out
	delayms(50);		//Delay 50ms
//-----Vop setting-----			
	Write(COMMAND,0xC0);		//Set Vop by initial Module
	Write(DATA, 0x09);		//Vop = 14.2V
	Write(DATA, 0x01);		// base on Module
//-----Set Register-----			
	Write(COMMAND,0xC3);		// Bias select
	Write(DATA,0x03);		// 1/9 Bias, base on Module
	Write(COMMAND,0xC4);		// Setting Booster times
	Write(DATA,0x07);		// Booster X 8
	Write(COMMAND,0xC5);		// Booster eff
	Write(DATA,0x01);		// BE = 0x01 (Level 2)
	Write(COMMAND,0xCB);		// Vg with booster x2 control
	Write(DATA,0x01);		// Vg from Vdd2
	Write(COMMAND,0xCC);		// ID1 = 00
	Write(DATA,0x00);		//
	Write(COMMAND,0xCE);		// ID3 = 00

ST7637

Write(DATA,0x00);		
Write(COMMAND,0xD0);		// Analog circuit setting
Write(DATA,0x1D);		//
Write(COMMAND,0xE7);		// low voltage mode setting
Write(DATA,0x22);		//
Write(COMMAND,0xE8);		//
Write(DATA,0x37);		//
Write(DATA,0x03);		//
Write(DATA,0x1F);		//
Write(COMMAND,0x3A);		// Color mode = 65k
Write(DATA,0x05);		//
Write(COMMAND,0x36);		// Memory Access Control
Write(DATA,0x00);		
Write(COMMAND,0xB0);		// Duty = 132 duty
Write(DATA,0x83);		
Write(COMMAND,0x20);		// Display Inversion OFF
1. Set Gamma table for Module, please refer spec setting.		
2. Set Temp compensation for Module, please refer spec setting.		
Write(COMMAND,0x2A);		// COL//
Write(DATA,0x00);		// 0~127
Write(DATA,0x7F);		
Write(COMMAND,0x2B);		// Page //
Write(DATA,0x00);		// 0~127
Write(DATA,0x7F);		
}		
void Set_OTP_Register(void)		
{		
//-----Set OTP register-----		
Write(COMMAND, 0xCD);		//ID2
Write(DATA, 0x80);		
Write(COMMAND, 0xB5);		// N-Line

ST7637

	Write(DATA, 0x03);		// RST, 4-line inversion
	Write(COMMAND,0xD0);		// Analog circuit setting
	Write(DATA,0x1D);		//
	Write(COMMAND,0xD7);		//Auto read Set
	Write(DATA,0x9F);		//OTPB Disable
	Write(COMMAND,0xB4);		//PTL Mode Select
	Write(DATA,0x18);		//PTLMOD → Normal Mode
	}		
	Note#1		
	void Fine_Tune_Vop(void)		
	{		
	//----- Show Map -----		
	Show_Image();		//Display a image
	//----- Display ON -----		
	Write(COMMAND, 0x29);		// Display On
	//-----Fine tune Vop offset-----		
	Write(COMMAND, 0xC1);		//Fine tuning Vop here by command
	or		0xc1(VopOffsetInc),0xc2(VopOffsetDec).
	Write(COMMAND, 0xC2);		
	Note#2		
	}		

	void OTP_Writing(void)		
	{		
	//-----Display OFF-----		
	Write(COMMAND, 0x28);		// Display Off
	Delaysms(50);		// delay 50ms
	//-----OTP writing-----		
	Write(COMMAND, 0x00D9);		// Keep Frame Rate
	Write(DATA, 0x0040);		//
	Write(COMMAND, 0x00E4);		//OTP,OTP selection
	Write(DATA, 0x0058);		// Select OTP
	Write(COMMAND, 0x00E5);		// Set OTP writing setup
	Write(DATA, 0x000C);		
	Write(COMMAND, 0x00E0);		// Read/write mode setting

ST7637

Write(DATA, 0x0020);		// Set Write mode
Delaysms(100);		// Delay 100ms
Write(COMMAND, 0x00E2);		// Write active
Delaysms(100);		// Delay 100ms
Write(COMMAND, 0x00E1);		// Cancel control
}		

void check program(void)		
{		
//-----disable autoread + Manual read once -----		
Write(COMMAND,0Xd7);		// Auto Load Set
Write(DATA,0x9f);		// Auto Load Disable
Write(COMMAND,0xE0);		// EE Read/write mode
Write(DATA,0x00);		// Set read mode
delaysms(10);		// Delay 10ms
Write(COMMAND,0xE3);		// Read active
delaysms(20);		// Delay 20ms
Write(COMMAND,0xE1);		// Cancel control
//----- Sleep OUT -----		
Write(COMMAND, 0x28);		// display off
Write(COMMAND, 0x11);		// Sleep Out
delaysms(50);		//Delay 50ms
//-----Vop setting-----		
Write(COMMAND,0xC0);		//Set Vop by initial Module
Write(DATA, 0x09);		//Vop = 14.2V
Write(DATA, 0x01);		// base on Module
//-----Set Register-----		
Write(COMMAND,0xC3);		// Bias select
Write(DATA,0x03);		// 1/9 Bias, base on Module
Write(COMMAND,0xC4);		// Setting Booster times
Write(DATA,0x07);		// Booster X 8
Write(COMMAND,0xC5);		// Booster eff
Write(DATA,0x01);		// BE = 0x01 (Level 2)
Write(COMMAND,0xCB);		// Vg with booster x2 control

ST7637

Write(DATA,0x01);		// Vg from Vdd2
Write(COMMAND,0xCC);		// ID1 = 00
Write(DATA,0x00);		//
Write(COMMAND,0xCE);		// ID3 = 00
Write(DATA,0x00);		
Write(COMMAND,0xD0);		// Analog circuit setting
Write(DATA,0x1D);		//
Write(COMMAND,0xE7);		// low voltage mode setting
Write(DATA,0x22);		//
Write(COMMAND,0xE8);		//
Write(DATA,0x37);		//
Write(DATA,0x03);		//
Write(DATA,0x1F);		//
Write(COMMAND,0x3A);		// Color mode = 65k
Write(DATA,0x05);		//
Write(COMMAND,0x36);		// Memory Access Control
Write(DATA,0x00);		
Write(COMMAND,0XB0);		// Duty = 132 duty
Write(DATA,0x83);		
Write(COMMAND,0x20);		// Display Inversion OFF
Write(COMMAND,0xF7);		// command for temp sensitivity.
Write(DATA,0x06);		//
3. Set Gamma table for Module, please refer spec setting.		
4. Set Temp compensation for Module, please refer spec setting.		
Write(COMMAND, 0x29);		// Display On
}		

void Gamma_Table(void)		
{		
Write(COMMAND,0xF9);		//
Write(DATA,0x00);		//
Write(DATA,0x02);		//

ST7637

Write(DATA,0x04);	//
Write(DATA,0x06);	//
Write(DATA,0x08);	//
Write(DATA,0x0A);	//
Write(DATA,0x0C);	//
Write(DATA,0x0E);	//
Write(DATA,0x10);	//
Write(DATA,0x12);	//
Write(DATA,0x14);	//
Write(DATA,0x16);	//
Write(DATA,0x18);	//
Write(DATA,0x1A);	//
Write(DATA,0x1C);	//
Write(DATA,0x1E);	//
}	

void Temp_Compensation(void)	
{	
Write(COMMAND,0xF0);	//frame frequency in temp
Write(DATA,0x06);	//45Hz (-30 [^] C ~ -10 [^] C)
Write(DATA,0x0B);	//60Hz (-10 [^] C ~ 0 [^] C)
Write(DATA,0x0D);	//72Hz (0 [^] C ~ 10 [^] C)
Write(DATA,0x12);	//77Hz (10 [^] C ~ 90 [^] C)
Write(COMMAND,0xF7);	//Temp Sensitivity Setting
Write(DATA,0x06);	//
Write(COMMAND,0xF4);	//TC Curve -0.06%
Write(DATA,0x33);	//
Write(DATA,0x33);	//
Write(DATA,0x33);	//
Write(DATA,0x33);	//
Write(DATA,0x33);	//
Write(DATA,0x33);	//
Write(DATA,0x33);	//
Write(DATA,0x33);	//
}	

Note:

- #1 *If the Vop and display performance is not suitable after burning OTP , the Vop has to refine tune.*
- #2 *In this section "+" & "-" key button, please execute Write(COMMAND,0xC1) to increase one step at Vop and execute Write(COMMAND,0xC2) to decrease one step at Vop, if necessary.*
- #3 *The TC is turn on in burning flow. If LCD module is too dark or bright, it's an effect of backlight.*

◆ **A6**- selection of application voltage

- Vop requirement: $[V_{dda} \times BS \times BE]$ Vop
- BS is Vop booster stage and BE is booster efficiency. Referential values are listed below: (assume $V_{dda}=2.8V$, Vop booster stage= $\times 8$)
n-line setting=0x00: BE=77%
n-line setting=0x01: BE=66%
n-line setting=0x06: BE=74%
actual BE should be determined by adding module loading and ITO resistance value.
- $V_{dda}<3V$: $3V \leq V_g \leq 2 \times V_{dda}$, $V_{dda} \geq 3V$: $1.8V \leq V_g \leq 2 \times V_{dda}$.
- $V_m = V_g/2$ and $0.7V < V_m < V_{dda} - 0.7V$.
- The worst condition should be considered:
Low temperature effect and display on with gray pattern on panel.

Referential LCD module setting

Condition: $V_{dda}=2.8V$, Vop booster stage= $\times 8$, booster level=level 2, duty=1/132, panel size=1.5"

bias	Vop (n-line=0x00)	Vop (n-line=0x01)	Vop (n-line=0x06)
1/10	15V~17.24V	14.78V	15V~16.57V
1/9	13.5V~17.24V	13.5V~14.78V	13.5V~16.57V

Note: it is recommended to reserve some range for user adjustment and temperature effect.

ST7637 Serial Specification Revision History		
Version	Date	Description
0.x		Preliminary version
1.0	2007/1/17	First issue
1.1	2007/03/10	<ol style="list-style-type: none">1. Modify Application Note example circuit ST7637 pad name2. Remove command B4h.3. Modify resolution value of example2 in vertical scroll example.
1.2	2007/4/30	<ol style="list-style-type: none">1. Specify OTP and OTPB register.2. Modify application note A1b and A1d.3. Modify application note A3 for abnormal power off.
1.3	2007/5/31	<ol style="list-style-type: none">1. Redefine the programming mechanism of non-volatility memory.2. Modify type error in command 0xC2h.
1.4	2007/10/04	<ol style="list-style-type: none">1. Specify relationship between Vg, Vdda and Vddi.2. Add application note for selection of application voltage.3. Redefine the value of sleep current.