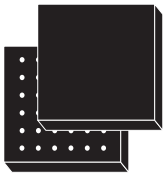
STw5094A

18-bit Low Power Asynchronous Stereo Audio DAC with Integrated Power Amplifiers and Voice Codec

FEATURES

- Complete stereo audio digital to analog converters and filters
  - 18-bit, 8 kHz to 48 kHz DAC with sample-rate conversion
  - Linear phase analog&digital filters
  - 16 Ω load stereo headphones drivers, 8 Ω load mono loudspeaker driver for group listening
- Stereo audio DAC features
  - Asynchronous sampling DAC: does not require oversampled clock and information on the audio data sampling frequency. Jitter tolerant
  - Multibit ΣΔ modulator with data weighted averaging DAC
  - 92 dB dynamic range, 0.01% THD over 16 Ω load performance
  - Support any sampling frequency in the range 8 kHz to 48 kHz
  - DSP functions for bass-treble-volume controls, deemphasis filter and dynamic compression
  - Tones from tone generator can be injected in the audio paths
- Stereo headphones and loudspeaker/earpiece power amplifiers features and stereo input for FM radio features:
  - 20 kHz bandwidth stereo headphones outputs. Driving capability: 40 mW (typ. 0.1% T.H.D) over 16 Ω with 40 dB range programmable gain
  - Balanced earpiece⁄ loudspeaker output. Driving capability: 300 mW (typ. 0.1% T.H.D) over 8 Ω with 30dB range programmable gain
  - Analog stereo input for FM radio with 38 dB range programmable gain



TFBGA 6x6 (36 pins)
ORDER CODES: STw5094AD/LF, STw5094ADT/LF

- Complete CODEC and filter system
  - 14-bit linear or 8-bit companded ADC and DAC
  - Transmit and receive digital band-pass filters
  - Active antialias and smoothing filters
  - 8 Ω load earpiece/loudspeaker driver, 16 Ω load auxiliary driver
- Voice CODEC features
  - Support 8 kHz or 16 kHz sampling rate
  - One microphone biasing output
  - Remote control function
  - Three switchable microphone amplifier inputs. 42.5 dB range programmable gain
  - Transient supression during power up and power down
  - Internal programmable sidetone
  - Internal ring, tone and dtmf generator
  - Programmable PWM buzzer driver
- General features
  - Single 2.7 V to 3.3 V supply
  - Extended temperature range operation [1] -40 °C to 85 °C
  - 1 µW standby power (typ. AT 2.7V).
  - 16 mW operating power in audio listening mode (typ. at 2.7 V).

1.Functionality guaranteed in the range -40°C to +85°C; Timing and Electrical Spec. are guaranteed in the range -30°C to +85°C.

- 11 mW operating power in voice codec mode (typ. at 2.7 V).
- 1.8 V to 3.3 V CMOS compatible digital interfaces
- Programmable PCM interface
- I^2C compatible control interface
- Programmable master/slave serial audio data input interface (I^2S and other formats)
- Frequency programmable clock output

APPLICATIONS

- CDMA,GSM,DCS1800,PCS1900,JDC digital cellular telephones with MP3 and FM radio stereo listening functions
- Portable devices with a stereo digital audio source and FM radio listening function

GENERAL DESCRIPTION

STw5094A is a low power asynchronous stereo audio DAC device with headphones amplifiers for high quality MP3 and FM radio listening. The STw5094A includes also an high performance low power combined PCM Codec/ filter tailored to implement the audio front-end functions required by low voltage low power consumption digital cellular terminals with added MP3 and FM radio listening.

The STw5094A registers are accessed through an I^2C-bus compatible interface.

The STw5094A asynchronous stereo audio DAC section is suited for MP3, or any other audio stereo source, listening. It supports any rate from 8 kHz to 48 kHz, can tolerate jitter on audio data and does not requires an oversampled clock. The audio data serial interface can be master or slave, it is I^2S compatible and supports other standard serial interface formats. The internal D to A converters work with 18 bit input resolution.

The stereo headphones drivers can also be used for FM radio listening via an auxiliary stereo analog input. A loudspeaker driver can also be used for monophonic group listening.

The STw5094A voice Codec section can be configured either as a 14-bit linear or as an 8-bit companded PCM coder. The frame voice Codec sample rate can be either the standard 8 kHz value or the extended 16 kHz one.

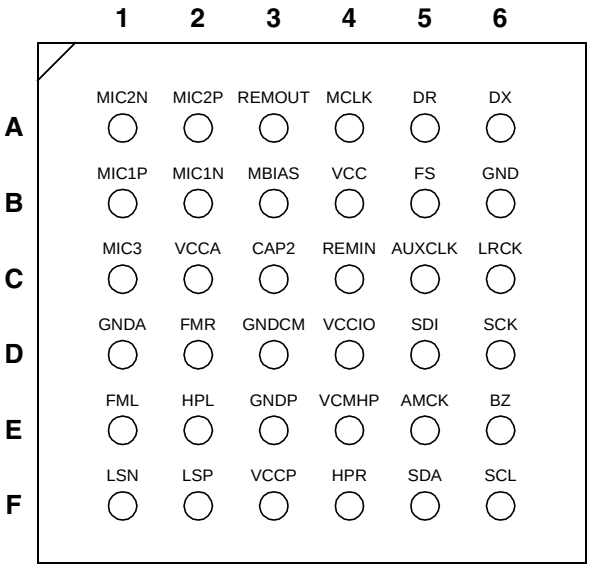
In addition to the stereo audio DAC and Codec/ filter functions, STw5094A includes a tone/ ring/ DTMF generator that can be used both in audio listening mode and in voice Codec mode, a sidetone generation, a buzzer driver output and a remote control function tailored to handle an external on-hook off-hook button. STw5094A Voice Codec fulfills and exceeds D3/ D4 and CCITT recommendations and ETSI requirements for digital handset terminals. The Stereo Audio DAC part fulfills and exceeds the requirements for MP3 quality and FM radio quality listening. Main applications include digital mobile phones with added low-power high-quality MP3 and/ or FM radio listening features, or any battery powered equipment that requires Stereo Audio DAC with Headphones drivers.

ORDER CODES

Part Number	Description
STw5094AD/LF	TFBGA 36 Tray
STw5094ADT/LF	TFBGA 36 Tape and Reel

TABLE OF CONTENT

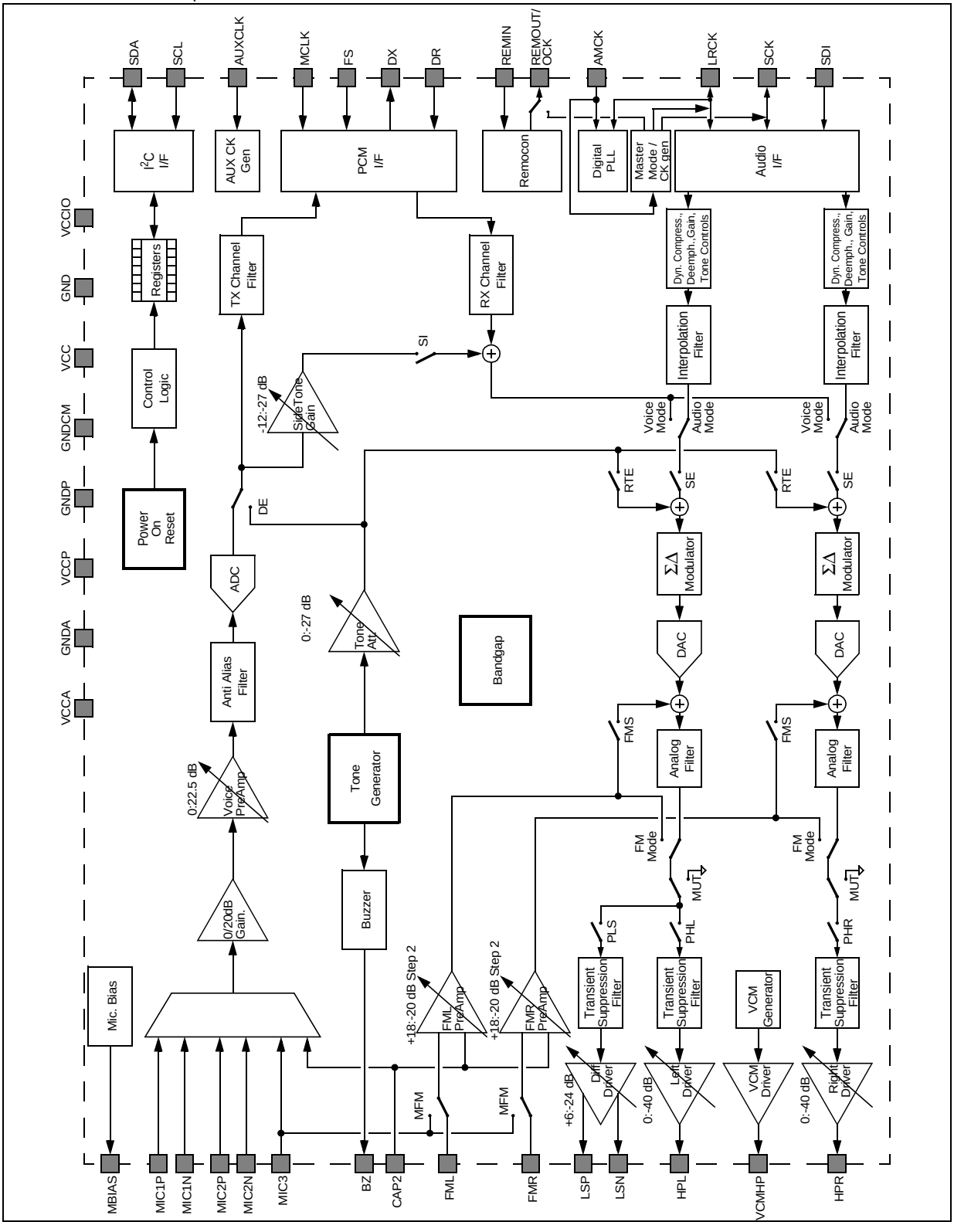
PIN CONNECTIONS (TOP VIEW)



TFBGA 6x6x1.2 (36 Pin)

FUNCTIONAL BLOCK DIAGRAM

Note: This diagram shows the functionality of the device and of some register bits but it does not necessarily reflect the exact hardware implementation



SIGNAL DESCRIPTION

Type definitions:

AI - Analog input, AO - Analog Output, DI - Digital Input, DO - Digital output, DOT - Digital Output Tristate, DIOD - Digital Input Output Open Drain, DIOT - Digital Input Output Tristate, P - Power Supply or Ground.

Pin N°	Name	Type	Description
B1	MIC1P	AI	Positive high impedance input to transmit preamplifier for microphone 1 connection.
B2	MIC1N	AI	Negative high impedance input to transmit preamplifier for microphone 1 connection.
A2	MIC2P	AI	Positive high impedance input to transmit preamplifier for microphone 2 connection.
A1	MIC2N	AI	Negative high impedance input to transmit preamplifier for microphone 2 connection.
C1	MIC3	AI	High impedance single ended input to transmit preamplifier for microphone 3 connection. MIC3 can be used as monophonic input for the FM path in place of FML and FMR
B3	MBIAS	AO	Microphone Biasing Switch.
E1	FML	AI	Auxiliary analog audio Left channel input.
D2	FMR	AI	Auxiliary analog audio Right channel input.
F2,F1	LSP, LSN	AO	Receive analog amplifier complementary outputs. This differential output can drive 50nF (with series resistor) or directly an earpiece transductor of 8Ω The signal at this output can be: the sum of the Receive Speech signal from DR, FML (or MIC3) input, the Internal Tone Generator and the Sidetone signal, or the sum of the Audio Left channel, FML (or MIC3) input and the Internal Tone Generator, or can come from FML (or MIC3) input.
E2	HPL	AO	Audio headphone amplifier Left channel output. This output can drive 50nF (with series resistor) or directly an earpiece transductor of 16Ω The signal at this output can be the sum of Audio Left channel, FML (or MIC3) input and Internal Tone Generator, or the sum of Receive Speech signal from DR, FML (or MIC3) input, Internal Tone Generator, Sidetone signal, or can come from FML (or MIC3) input.
F4	HPR	AO	Audio headphone amplifier Right channel output. This output can drive 50nF (with series resistor) or directly an earpiece transductor of 16Ω The signal at this output can be the sum of Audio Right channel, FMR (or MIC3) input and Internal Tone Generator, or the sum of Receive Speech signal from DR, FMR (or MIC3) input, Internal Tone Generator, Sidetone signal, or can come from FMR (or MIC3) input.
A3	REMOUT/OCK	DO	Remocon function digital output / Oversampled Clock out.
C4	REMIN	DI	Remocon function input. A high level at this pin is detected as a non pressed key, while a low level is detected as a pressed key.
E6	BZ	AO	Pulse width modulated buzzer driver output.
F6	SCL	DI	I2C-bus interface serial clock input. SCL is asynchronous with the other system clocks.
F5	SDA	DIOD	I2C-bus interface serial data input-output.
C6	LRCK	DIOT	Left／ Right clock or Frame Sync for Audio interface input in Slave mode, output in Master mode.
D6	SCK	DIOT	Audio interface Serial Clock input in Slave mode, output in Master mode.
D5	SDI	DI	Audio interface Data input.
E5	AMCK	DI	Master Clock Input for Audio Mode. Can also be used as Master Clock in Tone Only and FM Modes.

Pin N°	Name	Type	Description
A6	DX	DOT	Transmit Data output: Data is shifted out on this pin during the assigned transmit time slots. Elsewhere DX output is in the high impedance state. In delayed and non-delayed normal frame sync modes, voice data byte is shifted out from tristate output DX at the MCLK frequency on the rising edge of MCLK, while in non-delayed reverse frame sync mode voice data is shifted out on the falling edge of MCLK.
A5	DR	DI	Receive data input: Data is shifted in during the assigned Received time slots In delayed and non-delayed normal frame sync modes voice data byte is shifted in at the MCLK frequency on the falling edges of MCLK, while in non-delayed reverse frame sync mode voice data byte is shifted in on the rising edge of MCLK.
B5	FS	DI	Frame Sync input for Voice Mode: This signal is a 8／ 16kHz clock which defines the start of the transmit and receive frames. Any of three formats may be used for this signal: non delayed normal mode, delayed mode, and non delayed reverse mode.
A4	MCLK	DI	Master Clock Input for Voice Mode. Can also be used as Master Clock in Tone Only and FM Modes. The allowed clock frequencies are 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz. MCLK is the Voice Data Clock.
C5	AUXCLK	DI	Auxiliary Clock Input. Can be used as Master Clock in Tone Only and FM Modes. Allowed clock frequencies are 512kHz, 1.536MHz, 2.048MHz or 2.56MHz.
E4	VCMHP	AO	VCM Driver Output. Can be used as common mode node for HPL and HPR outputs.
C3	CAP2	AI	A capacitor must be connected between this node and Ground.
C2	VCCA	P	Power supply input for the analog section. VCC and VCCA can be directly connected together for low cost applications.
D1	GNDA	P	Analog Ground: All analog signals are referenced to this pin. GND and GNDA can be connected together for low cost applications.
F3	VCCP	P	Power supply input for the output drivers.
E3	GNDP	P	Power ground. Output drivers are referenced to this pin. GNDP and GNDA must be connected together.
D3	GNDCM	P	Analog Ground connection. GNDCM can be connected to GNDA.
B4	VCC	P	Power supply input for the digital section.
B6	GND	P	Ground for the digital section
D4	VCCIO	P	Power supply Input for the Digital I／ O pins.

FUNCTIONAL DESCRIPTION

1 DEVICE MODES

STw5094A can work in 4 different modes, selected by bits **MD** in Control Register 21 (**CR21**). Depending on the mode different data interfaces, clock inputs, and internal blocks are selected. A built-in power consumption management function keeps in power down the blocks that are not needed by the selected operating mode. In all the modes the Output Drivers can be activated in different combinations with bits **PLS**, **PHL**, **PHR** in **CR6** (in case of stereo input and **LSP**/ **N** driver selected the Left channel is sent to this driver, while in case of voice input and **HPL** + **HPR** drivers selected the same signal is sent to both drivers).

1.1 Audio Mode

In Audio mode the path from the Audio interface (Au I/ F) to the output drivers is active to allow the Stereo Audio DAC function. The Au I/ F is active while the PCM I/ F is inactive.
The master clock of the device is **AMCK**. The **AMCK** frequency is fixed, and independent from the audio samples data rate (**LRCK** frequency). **AMCK** source can be any fixed system clock whose nominal frequency value lies in the range 9.5MHz to 28MHz (the full range is covered in three sub-ranges, selected by bits **AMCK_DIV** in **CR18**). The rate of the audio data (**LRCK** frequency) can be any value in the range 8kHz to 48kHz (non standard values are allowed) and does not need to be specified.

Since the **AMCK** clock is used directly in the D to A Converters section, its jitter and spectral properties must be adequate to the desired Audio quality.

In Audio Mode there are additional functions for audio signal processing:

– A digital volume control with 54 dB range is implemented (bits **VOL** in **CR20**). If the digital volume is used in addition with the analog gain regulation a 94dB range volume is obtained.
– Bass controls can be regulated in the -12.5dB to +12.5dB range in 2.5 dB step (bits **BASS** in **CR19**).
– Treble controls can be regulated in the -6dB to +6dB range in 2 dB step (bits **TREBLE** in **CR19**).
– The 50µs/ 15µs de-emphasis filter is activated instead of treble controls (bits **TREBLE** in **CR19**). Note: the time constants are referred to the 44.1kHz FS.
– A dynamic range compressor is implemented (bit **CMP** in **CR20**).

Note: The de-emphasis filter and the Bass/Treble controls freq. responses scale with the input sampling rate.

The tone/ ring/ DTMF generator can be activated if needed. In audio mode the frequency values of the tones is a function of the **AMCK** frequency value as explained in Table 1.

1.2 Voice Mode

In Voice mode the TX path from microphone input to **DX** and the RX path from **DR** to the output drivers are active to allow the PCM CODEC function. The PCM I/ F is active while the Au I/ F is inactive.
The master clock of the device is **MCLK**, the frequency of the clock can be selected with bits **F** in **CR0**.
The tone/ ring/ DTMF generator can be activated if needed.

1.3 Tone Only Mode

In tone only mode the path from the tone generator to the output drivers and to the buzzer is active to allow tones or ringer listening only. Both Au I/ F and PCM I/ F are inactive, as all the Audio and Voice converters functions.

The master clock of the device can be selected to be **AUXCLK**, **MCLK** or **AMCK** (bits **CFM** in **CR21**).

1.4 FM Mode

In FM mode the path from **FML** and **FMR** analog inputs to the output Drivers is active to allow FM Stereo Radio listening. Both Au I/ F and PCM I/ F are inactive, as all the Audio and Voice converters functions.
The master clock of the device can be selected to be **AUXCLK**, **MCLK** or **AMCK** (bits **CFM** in **CR21)**.
The Tone/ Ring/ DTMF generator is in power down.

2 DEVICE OPERATION

2.1 Power on Initialization, Software Reset

When power is first applied, the “power on reset” circuitry initializes STw5094A and puts it into the power down state. All the Registers are initialized as indicated in the Control Register description section. All the functions are disabled.
The registers can also be initialized to the default state by writing bit **SRS** (software reset) in **CR21.**

2.2 Power up/ down control

It is recommended that all programmable functions (excluding the gain controls, bass-treble controls and dynamic compression function) are set while the device is powered down. Power state control can then be included in the last programming instruction (the power up bit **PU** is located in the last address register (**CR21**) so that the multi-byte mode of the control interface can be easily used to program all the required functions before power up).
When a power up command is given, all the circuits needed for the selected mode are activated (in Voice mode the **DX** output will remain in the high impedance state until the second **FS** pulse after power up arrives). A built-in power consumption management function keeps in power down the blocks that are not needed by the selected operating mode.

2.3 Power down state

Following a period of activity, power down state may be reentered by writing 0 in bit **PU** in **CR21**. All the Control Registers remain in their current state and can be changed by I^2C control interface.
In addition to the power down instruction, the detection of absence of the current Master Clock (no transition detected) automatically puts the device in power down state without setting bit **PU**. If transitions on the master clock are detected the device is put again in power up.

2.4 Voice Transmit section

This section is active in Voice Mode. Voice Transmit analog preamplifier gain is designed in two stages to enable gains up to 42.5 dB. Stage 1 provides a selectable 0 or 20 dB gain via bit **PG** in **CR4**. Stage 2 is a programmable gain amplifier which provides from 0 to 22.5 dB of additional gain in 1.5dB step. It can be programmed with bits **TXA** in **CR4**. Three microphone inputs are provided, two differential (**MIC1P/ N, MIC2P/ N**) and one single ended (**MIC3**). They may also be used connect an auxiliary audio circuit. The microphone input or Transmit Mute is selected with bits **MS** in **CR4**. In the Mute case, the analog transmit signal is grounded. A separate **MBIAS** output can be used to bias a microphone (bit **MB** in **CR4**). An active anti-alias filter then precedes the single bit $\Sigma\Delta$ analog to digital converter that is followed by an 8th order IIR digital TX channel filter. The TX channel filter is band-pass if the **FS** frequency is 8kHz and low-pass if the **FS** frequency is 16kHz (bit **VFS** in **CR0**). A precision on chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the analog blocks is cancelled by an internal autozero circuit. Voice data is sent to the PCM I/ F to be serially sent to **DX** output.

2.5 Voice Receive section

This section is active in Voice Mode. Voice Data coming from PCM I/ F **DR** pin is sent to the 8th order digital IIR RX channel filter. The filter can be selected to be band-pass or low-pass, with bit **HPB** in **CR5**, when **FS** frequency is 8kHz, while it is always low-pass when **FS** frequency is 16kHz. The filter is followed by a $\Sigma\Delta$ digital to analog converter and a 3rd order switched-capacitor reconstruction filter. The Sidetone can be summed to the received signal (bit **SI** in **CR5**) and its amplitude can be programmed with bits **SA** in **CR5**.

2.6 Stereo Audio DAC section

This section is active in Audio Mode. The Left and Right Audio samples coming from the Audio Interface are interpolated with an FIR filter and synchronized to the **AMCK** clock in order to feed the oversampled multi-bit $\Sigma\Delta$ modulator, the digital to analog converter is followed by a 3^{rd} order switched-capacitor reconstruction filter.

2.7 FM Input Path

The device is provided with stereo and mono single ended analog inputs, designed to amplify analog signals from an FM decoder but they can be considered as generic analog inputs. The stereo analog inputs are **FML** and **FMR** pins, or alternatively **MIC3** pin for mono input (sent to left and right channels). The selection between **FML**-**FMR** or **MIC3** is done with bit **MFM** in **CR20**.
The analog inputs are connected to a programmable gain stage that can amplify the signals in the range -20dB to +18dB in 2 dB steps. The gain control is independent for Left and Right channel and is selected with bits **FMLA** in **CR10** (Left) and bits **FMRA** in **CR11** (Right).

There are 2 ways to connect the FM inputs to the output drivers. The first is to select the FM Mode (bits **MD** in **CR21**). The second is to activate Audio or Voice or Tone Only modes and to set to 1 bit **FMS** in **CR20**. In the last case the signal coming from FM inputs will be summed to the Audio or Voice or Tones signals respectively.

2.8 Output Drivers section

There are 3 Analog Output Drivers. The **LSP**／ **N** differential driver delivers 300mW typical power with 0.1% T.H.D. (250mW minimum undistorted) on a 8Ω earpiece／ loudspeaker (piezoceramic loads up to 50nF can also be driven with a series resistor), it has a 30dB range gain control (bits **LSA** in **CR7**). The 2 single ended drivers (**HPL** and **HPR**) deliver 40mW typical power with 0.1% T.H.D. (30mW minimum undistorted) on 16Ω stereo headphones, they have a 40dB range gain control (**CR8** for **HPL** and **CR9** for **HPR**). It is possible to put the drivers in power-down and in power-up by programming bits **PLS**, **PHL**, **PHR** in **CR6**. These settings are not dependent from the selected operative Mode.
The common mode voltage of all the drivers is selected with bits **VCL** in **CR18** in the range 1.2V to 1.65V with 150mV steps. This feature is useful to set the common mode voltage to VCCP/2 and therefore to extend the output range and increase the output power.

If **HPL** and **HPR** are enabled together in Voice Mode or Tone Only Mode the same signal is sent to both Drivers. The active Drivers can be muted (keeping them in power-up state) using bit **MUT** in **CR6**. At power-up or after a change in **PLS** or **PHL** or **PHR** bits the outputs are muted for 10 ms to avoid unwanted noise. The transient suppression filter is used to avoid clicks when the gain value is changed.

2.9 Common Mode Driver

The common mode voltage driver (**VCMHP** pin) simplifies the application for a stereo headset connection saving two decoupling capacitors in series with HPL and HPR. The loads of the single ended drivers are connected on one side to **HPL** and **HPR** respectively, and on the other to **VCMHP**, that has the same common mode voltage. The driver is enabled with bit **VCE** in **CR18**.
The output voltage of **VCMHP** is selected with bits **VCL** in **CR18** in the range 1.2V to 1.65V with 150mV steps.

2.10 Tone Generator

The Tone Generator can be activated (writing **CR12**) in all the STw5094A operating modes except FM mode. In Voice and Audio modes the tones are summed to the signal. It is possible to generate 1 or 2 summed waveforms (either sinusoidal or square wave), their frequencies can be set in **CR13** for the first one (f1) and in **CR14** for the second one (f2) accordingly to the values listed in Table 1 if the active master clock is **MCLK** or **AUXCLK**. If the active master clock is **AMCK** the frequency values specified in Table 1 must be multiplied by a factor k_{fAMCK} that depends on the **AMCK** frequency value. The amplitude of the generated waveform can be regulated in **CR12** over a 33dB range. When both f1 and f2 are selected the amplitude of f1 and f2 are lowered by 5dB and 7dB respectively with respect to the amplitude of a single waveform. In this way the amplitude of the summed waveforms does not overload and there is a 2dB difference between f1 and f2 amplitude as required for DTMF generation. The Tone Generator output can be sent to the Voice Transmit section (in Voice Mode), to the Power amplifiers, possibly mixed with audio or voice, (in all the modes except FM mode) and to the buzzer output **BZ** (in all the modes except FM mode).

2.11 Buzzer Output

The output **BZ** is intended to drive a Buzzer, via an external BJT, with a squarewave pulse width modulated (PWM) signal. The frequency of the signal is stored in **CR13** (see Tone Generator section and Table 1 for frequency values). For some applications it is also possible to multiply this PWM signal with a squarewave signal having a frequency stored in **CR14**. The duty cycle of the buzzer output can be varied in **CR15** in order to change the buzzer volume. Maximum load for **BZ** is 5kΩ and 50pF

2.12 Voice Data Interface (PCM I/F)

The PCM I/F is used to exchange the Voice data in both TX and RX direction, it can be programmed for linear format data or companded A-law or μ-law format (see Fig.1, 2 and 3).
Frame Sync input **FS** determines the beginning of frame. It may have any duration from a single cycle of **MCLK** to a squarewave. Three different relationships may be established between the Frame Sync input and the first time slot of the frame by setting bits **DM** in **CR1**. In non delayed normal and reverse data mode (long frame timing) the first time slot starts at the rising edge of FS. In delayed data mode (short frame sync timing) **FS** input must be high for at least a half cycle of **MCLK** before the frame start.

When linear code is selected (bit **CM** = 0 in **CR0**) the MSB is transmitted and received first, the word length is 16 bit. When companded code is selected (bit **CM** = 1 in **CR0**) a time slot assignment may be used in all timing modes (bit **TS** in **CR1**), that allows connection to one of the two B1 and B2 voice data channels. Two data formats are available: in Format 1, time slot B1 corresponds to the 8 **MCLK** cycles that immediately follow the rising edge of **FS**, while time slot B2 corresponds to the 8 **MCLK** cycles that immediately follow time slot B1. In Format 2, time slot B1 is identical to Format 1 while time slot B2 appears two bit slots after time slot B1. This two bits space is left available for insertion of the D channel data. Data format is selected by bit **FF** in **CR0**.

Bit **EN** in **CR1** enables or disables data transfer on **DX** and **DR**.

Outside the selected time slot **DX** is in the high impedance condition. During the selected time slot the **DX** output and the **DR** input are synchronized as follow:

-If delayed or non-delayed modes are selected the transmit voice data is sent to **DX** output on the rising edges of **MCLK** and receive voice data is read at **DR** input on the falling edges of **MCLK**.

-If non-delayed reverse mode is selected the transmit voice data register is sent to **DX** output on the falling edges of **MCLK** and receive voice data is read at **DR** input on the rising edges of **MCLK.**

When 16kHz Frame Sync frequency is selected (bit **VFS** in **CR0**) the RX and TX filters are both low-pass and their cutoff frequencies are doubled.

It is possible to access the B channel data when companded A-law or μ-law formats are used (bits **MX** and **MR** in **CR1**). A byte written into **CR3A** will be sent to **DX** output in place of the transmit channel PCM data. A byte written in **CR2A** will be sent to the receive path. The current byte received on **DR** input can be read in **CR2A**.

2.13 Audio Data Interface (Au I/F)

The Au I/F is used to receive the Stereo Audio data. The pins related to the Au I/F are: the frame synchronism or Left/Right indicator **LRCK**, the serial bit clock **SCK**, and the serial data input **SDI**. **LRCK** and **SCK** can be input or output depending if the Au I/F is configured in Slave or Master mode.

The interface can be configured in 5 different modes programming bits **SPIM**, **MSM** and **DSPM** in **CR17**. In each mode different parameters (word length, signal polarity etc.) can be set writing **CR16.**

The **MSM** bit selects if Au I/F is Master or Slave. When **MSM**=0 the Au I/F is Slave: the serial bit clock **SCK** and the frame sync **LRCK** are input to the device. When **MSM**=1 the Au I/F is Master: **SCK** and **LRCK** are generated inside the device. The frequency of **LRCK** is programmed in **CR2B** and **CR3B** while its shape and the frequency of **SCK** change automatically with the selected mode (see paragraph below). Master mode is not available when the Au I/F is configured in SPI-mode (**SPIM**=1) regardless of the value of **MSM**.

The 5 possible mode modes are:

I^2S-Mode Slave (**SPIM**=0, **MSM**=0 and **DSPM**=0**)** in this mode the Au I/F is I^2S compatible (see Fig. 5 and 10) and the bit clock **SCK** and the left/right indicator **LRCK** signals are input to the device. **SCK** must have 16 periods per channel in case of 16bit data word and 32 periods per channel in case of 18bit to 24bit data word. **SCK** can be either a continuous clock or a sequence of bursts.

I²S-Mode Master (**SPIM**=0, **MSM**=1 and **DSPM**=0**)** this mode is functionally equivalent to I²S-mode Slave (see Fig. 7 and 10) but the bit clock **SCK** and the left/right indicator **LRCK** signals are generated by the device. **SCK** is generated with 16 periods per channel in case of 16bit data word and 32 periods per channel in case of 18bit to 24bit data word

DSP-Mode Slave (**SPIM**=0, **MSM**=0 and **DSPM**=1**)** in this mode the Au I⁄ F starting from a frame sync pulse on **LRCK** receives the Left and Right data one after the other (see Fig. 6 and 11). **SCK** is a free running bit clock: between 2 successive frame sync pulse there can be any number of SCK periods from the minimum necessary to transfer all the data bits up to the max. frequency limit specified for **SCK**. DSP-mode is suited to interface with a Master Multi-Byte Serial Interface.

DSP-Mode Master (**SPIM**=0, **MSM**=1 and **DSPM**=1**)** this mode is functionally equivalent to DSP-mode Slave but **LRCK** and **SCK** signals are generated by the device (see Fig. 8 and 12). **SCK** is generated with 32 periods per frame sync. in case of 16bit data word and 64 periods per frame sync. in case of 18bit to 24bit data word. DSP-mode Master is suited to interface with a Slave Multi-Byte Serial Interface.

SPI-Mode (**SPIM**=1 and **DSPM**=0**)** in this mode Left and Right data are received with separate data burst. Every burst is identified with a low level on **LRCK** signal (see Fig. 9 and 13). There is no timing difference between the Left and Right data burst: the two channels are identified by the fact that the first burst after Audio mode power-up identifies the Left channel data and the second one is the Right channel data and then Left and Right data repeat one after the other. **SCK** must have 16 periods per channel in case of 16bit data word and 32 periods per channel in case of 18bit to 24bit data word. SPI-mode can only be Slave: when **SPIM**=1 the values written on **MSM** is disregarded while **DSPM** must be set to 0.

In some of the above listed modes not all the combinations of the bits in **CR16** are available or meaningful:

- In DSP-Mode MSB is always received first (bit **ORD**=0), data word justification and **LRCK** polarity have no meaning.
- In SPI-mode the data word must be always left-justified (bit **DIF**=0) and non-delayed (bit **FOR**=1) and **LRCK** polarity must be always set for Left=0 (**INV**=0).

The audio data sample rate (**LRCK** frequency) can be any value in the range 8kHz to 48kHz**.**
Left channel data are always received first.
The first 35 Data frames after power up are discarded while the interpolation filters data memory is cleared.

2.14 LRCK & SCK generation in Master Mode

Setting **MSM**=1 and **SPIM**=0 in **CR17** enables the internal generation of the frame synchronism clock **LRCK** and of the serial bit clock **SCK**.

These clocks are obtained by variable division from the **AMCK** system clock. Given the **AMCK** frequency (f_{AMCK}), the desired sample rate frequency (f_{LRCK}) is obtained by writing in **CR2B** the least significant byte and in **CR3B** the most significant byte of the16bit integer result calculated with the following formula:

$$N = round(2^{23} \cdot (f_{LRCK} / f_{AMCK}))$$

The precision of the obtained f_{LRCK} is always better than ±1.7Hz.

The shape of **LRCK** waveform and the number of **SCK** periods for each **LRCK** period is set automatically depending on the values of bit **DSPM** in **CR17** and of **CR16** content (see Fig. 7,8,10 and 12).

Since **CR2B** and **CR3B** are overlaid registers, In order to write the division factor N in **CR2B** and **CR3B** the master mode must be selected in advance by setting **MSM**=1.

NOTE: LRCK and **SCK** are part of the Au I⁄ F, but Master mode generation can also be used as Frame Sync and Master clock in Voice Mode by connecting them to **FS** and **MCLK** (in this case a fixed clock on **AMCK** is needed).

Example: The master clock frequency is f_{AMCK}=12MHz, the required sampling frequency is f_{LRCK}=44.1kHz, N value is:

$$N = round(2^{23} \cdot (44100 / 12000000)) = 30828$$

30828 decimal corresponds to 786C hex so **CR2B** and **CR3B** must be loaded with 6C hex and 78 hex respectively, the frequency of **LRCK** will then be:

$$f_{LRCK} = (30828 \cdot 12000000\ Hz) / 2^{23} = 44099.8\ Hz.$$

2.15 OCK output clock generation

Setting **OCE** = 1 and **SPIM** = 0 in **CR17** enables the internal generation of the clock **OCK** on the pin **REMOUT/ OCK**. The clock output can be used as master clock for a digital device that provides the Audio Data to STw5094A.

This function is compatible with both Master mode and Slave mode of the **Au I/ F** and can be used in Normal mode and in DSP mode while it cannot be used in SPI mode. It can be activated also in Voice mode (provided the **AMCK** clock is available).

Because **OCK** clock is obtained by variable division from the master clock **AMCK, OCK** cannot have a frequency higher than the **AMCK** master clock frequency.

When **OCK** frequency is comprised between **AMCK** frequency and half the **AMCK** frequency **OCK** is obtained removing pulses, as evenly spaced as possible, from **AMCK** and thus reducing the frequency to the programmed value. When **OCK** frequency is lower than half **AMCK** frequency it is obtained by division on the rising edge of **AMCK**.

OCK polarity can be inverted setting **ROI**=1 in **CR17**.

OCK in Master Mode: when the **Au I/ F** is used in Master Mode the **OCK** frequency is 256 times the sampling frequency programmed in **CR2B** and **CR3B** using the formula described in Section 2.14 ($f_{OCK} = 256 \cdot f_{LRCK}$).

OCK in Slave Mode: when the **Au I/ F** is used in Slave Mode the **OCK** frequency can be set to any value (lower than **AMCK** frequency) and it is not related to the incoming **LRCK** frequency, then not limited to 256 oversampling. In this case to obtain the desired **OCK** frequency the following formula can be used:

$$N = round(2^{15} \cdot (f_{OCK} / f_{AMCK}))$$

where f_{OCK} is lower than f_{AMCK} (this corresponds to the fact that N cannot be greater than 7FFF hex).

Example: The master clock frequency is f_{AMCK}=19.2MHz, the oversampling factor is 384 and the sampling rate is 44.1 kHz, then the required **OCK** frequency is
f_{OCK} = 384 · 44.1 kHz = 16934400 Hz.

The value of N is:

$$N = round(2^{15} \cdot (16934400 / 19200000)) = 28901$$

28901 decimal corresponds to 70E5 hex so **CR2B** and **CR3B** must be loaded with E5 hex and 70 hex respectively, the frequency of **OCK** will then be

$$f_{OCK} = (28901 \cdot 19200000\ Hz) / 2^{15} = 16934179.7\ Hz = 384 \cdot 44099.4\ Hz$$

The **OCK** output clock function is alternative to the Remocon function because both share the same output pin: setting **OCE** = 1 will disable the Remocon function on the **REMOUT/ OCK** but the REMOCON output status will still be available reading bit **RDL** in **CR17** (see paragraph II.18 for more details on REMOCON function).

Since **CR2B** and **CR3B** are overlaid registers, in order to write the division factor N in **CR2B** and **CR3B**, the output clock function must be selected in advance by setting **OCE** = 1.

2.16 Control Interface (I^2C I/F)

The I^2C I/F is used to program the device by writing and reading the control registers (see Fig. 14 and 15). The interface is I^2C bus compatible, being the STw5094A a Slave device. **SDA** is the bidirectional open-drain data pin and **SCL** is the input clock pin. The Device Address is E2 hex. for writing and E3 hex. for reading.
The interface has an internal address register that keeps the current address of the control register to be read or written. At each write access of the interface the address register is loaded with the data of the register address field. The value in the address register is increased after each data byte read or write. It is possible to access the interface in 2 modes: single-byte mode in which the address and data of a single register are specified, and multi-byte mode in which the address of the first register to be written or read is specified and all the following bytes exchanged are the data of successive address registers starting from the one specified (in multi-byte mode the internal address counter restart from register 0 after the last register 21). Using the multi-byte mode it is possible to write or read all the registers with a single access to the device on the I^2C bus.

The Control interface can be used both in power-up and power-down state.

2.17 Master clock in FM mode and tone only modes

In FM mode and in Tone Only mode the Master Clock of the device can be selected to be **AUXCLK**, **MCLK** or **AMCK** writing bits **CFM** in **CR21**. The Auxiliary clock **AUXCLK** can be used when the Audio mode clock **AMCK** and the Voice mode clock **MCLK** are not available. **AUXCLK** and **MCLK** frequency selection is done with bits **F** in **CR0**.

2.18 REMOCON function

The REMOCON (Remote Control) function can be used to detect the status of an headset button. The REMOCON function is enabled by setting bit **REN** in **CR17**. If enabled, this function is active also when the STw5094A is in power-down state. The **REMOUT/OCK** pin is the output pin for the REMOCON function only if **OCE** = 0 in **CR17** (Section 2.15).

A High level at **REMIN** input is detected as a non pressed button, while a low level is detected as a pressed button. The "Pressed Button" information can be treated in 2 ways depending on bit **RLM** in **CR17**:

-if **RLM** = 0 (Transparent mode) the information at **REMIN** is seen at **REMOUT/OCK** after a debounce time of 50ms maximum;

-if **RLM** = 1 (Latched Mode) the information stored in bit **RDL** in **CR17** is seen at **REMOUT/OCK**. **RDL** is set after a debounce time of 50ms maximum when a low level at **REMIN** is detected. **RDL** is reset with power on initialization and can also be reset writing 0 in bit **RDL**.

The **REMOUT/OCK** output polarity can be inverted setting bit **ROI** in **CR17**: the pressed button information is presented at **REMOUT/OCK** output as a logic 1 if bit **ROI** = 0. If **ROI** = 1 the polarity is inverted.

PROGRAMMABLE REGISTERS

Control Register CR0 Functions (Address: 0x00)

7	6	5	4	3	2	1	0	Function
F(1:0)		VFS	CM	MA	IA	FF	B7	
0 0 1 1	0 1 0 1							MCLK or AUXCLK = 512 kHz * MCLK or AUXCLK = 1.536 MHz MCLK or AUXCLK = 2.048 MHz MCLK or AUXCLK = 2.560 MHz
		0 1						Voice Data Fs is 8 kHz * Voice Data Fs is 16 kHz
			0 1					Linear code * Companded code
								Linear Code / Companded Code
				0 0 1 1	0 1 0 1			2-complement * / μ-law: CCITT D3-D4 * sign and magnitude / μ-law: Bare Coding 2-complement / A-law including even bit inversion 1-complement / A-law: Bare Coding
						0 1		B1 and B2 consecutive (1) * B1 and B2 separated (1)
							0 1	8 bits time-slot (1) * 7 bits time-slot (1)

(1): significant in companded mode only
*: state at power on initialization

Control Register CR1 Functions (Address: 0x01)

7	6	5	4	3	2	1	0	Function
DM(1:0)			MR	MX	EN	TS	DL	
0 1 1	X 0 1							delayed data timing * non-delayed normal data timing non-delayed reverse data timing
		X						
			0 1					D_R connected to RX path * CR2A connected to RX path (1)
				0 1				TX path connected to D_X * CR3A connected to D_X (1)
					0 1			PCM I/F disabled * PCM I/F enabled
						0 1		B1 channel selected * B2 channel selected (1)
							0 1	Normal operation * Digital Loopback (Data from DR is sent to DX with 1 frame delay)

(1) significant in companded mode only
*: state at power on initialization
X: reserved: write 0

Control Register CR2A Functions (Address: 0x02) (Active when MSM=0 and OCE=0 in CR17)

7	6	5	4	3	2	1	0	Function
DRD(7:0)								
msb							lsb	Data sent to Receive path or Data received from DR input (1)

(1) Significant in companded mode only. CR2A is available only if Master mode and OCK out in CR17 are not enabled (MSM=0 and OCE=0).

Control Register CR2B Functions (Address: 0x02) (Active when MSM=1 or OCE=1 in CR17)

7	6	5	4	3	2	1	0	Function
DIVL(7:0)								
msb							lsb	Least significant byte of the frequency division factor for LRCK,SCK and OCK generation. (1)

(1) CR2B is available only if the Master mode or OCK out in CR17 are enabled (MSM=1 or OCE=1, and SPIM=0).

Control Registers CR3A Functions (Address: 0x03) (Active when MSM=0 and OCE=0 in CR17)

7	6	5	4	3	2	1	0	Function
DXD(7:0)								
msb							lsb	DX data transmitted (1)

(1) Significant in companded mode only. CR3A is available only if Master mode and OCK out in CR17 are not enabled (MSM=0 and OCE=0).

Control Registers CR3B Functions (Address: 0x03) (Active when MSM=1 or OCE=1 in CR17)

7	6	5	4	3	2	1	0	Function
DIVH(7:0)								
msb							lsb	Most significant byte of the frequency division factor for LRCK, SCK and OCK generation. (1)

(1) CR3B is available only if the Master mode or OCK out in CR17 are enabled (MSM=1 or OCE=1, and SPIM=0).

Control Register CR4 Functions (Address: 0x04)

7	6	5	4	3	2	1	0	Function
MS(1:0)		MB	PG	TXA(3:0)				
0 0 1 1	0 1 0 1							Transmit input muted * MIC1 Selected MIC2 Selected MIC3 Selected
		0 1						MBIAS output disabled * MBIAS output enabled
			0 1					20dB preamplifier gain * 0dB preamplifier gain
				0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1	0 dB Transmit Amplifier gain * 1.5 dB Transmit Amplifier gain Transmit Amplifier in 1.5 dB step 22.5 dB Transmit Amplifier gain

*: state at power on initialization

Control Register CR5 Functions (Address: 0x05)

7	6	5	4	3	2	1	0	Function
		HPB	SI	SA(3:0)				
X	X							
		0 1						Voice Codec Receive High Pass filter enabled (1) * Voice Codec Receive High Pass filter disabled
			0 1					Voice Codec internal sidetone disabled * Voice Codec internal sidetone enabled
				0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1	-12.5 dB Sidetone gain * -13.5 dB Sidetone gain Sidetone gain in 1 dB step -27.5 dB Sidetone gain

(1): Valid only when Voice Data Fs=8kHz (VFS=0). When Voice data Fs=16kHz (VFS=1) The High Pass Filter is always disabled.
*: state at power on initialization
X: reserved: write 0

Control Register CR6 Functions (Address: 0x06)

7	6	5	4	3	2	1	0	Function
		MUT	PLS	PHL	PHR	SE	RTE	
X	X							
		0 1						The active output Drivers are operative * The active output Drivers are muted
			0 1					LSP／ N output Driver is in power down * LSP／ N output Driver is in power up.
				0 1				HPL output Driver is in power down * HPL output Driver is in power up
					0 1			HPR output Driver is in power down * HPR output Driver is in power up
						0 1		Audio or Voice Codec Signal to LS or HP disabled * Audio or Voice Codec Signal to LS or HP enabled.
							0 1	Ring／ Tone to LS or HP disabled * Ring／ Tone to LS or HP enabled.

*: state at power on initialization
X: reserved: write 0

Control Register CR7 Functions (Address: 0x07)

7	6	5	4	3	2	1	0	Function
				LSA(3:0)				
X	X	X	X					
				0 0 0 0 - 1	0 0 0 0 - 1	0 0 1 1 - 1	0 1 0 1 - 1	Earpiece／ Loudspeaker Amplifier 6 dB gain Earpiece／ Loudspeaker Amplifier 4 dB gain Earpiece／ Loudspeaker Amplifier 2 dB gain Earpiece／ Loudspeaker Amplifier 0 dB gain * Earpiece／ Loudspeaker Amplifier gain in 2 dB step Earpiece／ Loudspeaker Amplifier -24 dB gain

*: state at power on initialization
X: reserved: write 0

Control Register CR8 Functions (Address: 0x08)

7	6	5	4	3	2	1	0	Function	
			HPLA(4:0)						
X	X	X							
			0	0	0	0	0	Headphones amplifier (Left channel) 0 dB gain	
			0	0	0	0	1	Headphones amplifier (Left channel) -2 dB gain	
			0	0	0	1	0	Headphones amplifier (Left channel) -4 dB gain	
			0	0	0	1	1	Headphones amplifier (Left channel) -6 dB gain	*
			-	-	-	-	-	Headphones amplifier (Left channel) gain in 2 dB step	
			1	0	1	0	0	Headphones amplifier (Left channel) -40 dB gain	

*: state at power on initialization
X: reserved: write 0

Control Register CR9 Functions (Address: 0x09)

7	6	5	4	3	2	1	0	Function	
			HPRA(4:0)						
X	X	X							
			0	0	0	0	0	Headphones amplifier (Right channel) 0 dB gain	
			0	0	0	0	1	Headphones amplifier (Right channel) -2 dB gain	
			0	0	0	1	0	Headphones amplifier (Right channel) -4 dB gain	
			0	0	0	1	1	Headphones amplifier (Right channel) -6 dB gain	*
			-	-	-	-	-	Headphones amplifier (Right channel) gain in 2 dB step	
			1	0	1	0	0	Headphones amplifier (Right channel) -40 dB gain	

*: state at power on initialization
X: reserved: write 0

Control Register CR10 Functions (Address: 0x0A)

7	6	5	4	3	2	1	0	Function	
			FMLA(4:0)						
X	X	X							
			0	0	0	0	0	FM Preamplifier (Left channel) +18 dB gain	
			0	0	0	0	1	FM Preamplifier (Left channel) +16 dB gain	
			-	-	-	-	-	FM Preamplifier (Left channel) gain in 2 dB step	
			0	1	0	0	1	FM Preamplifier (Left channel) 0 dB gain	*
			-	-	-	-	-	FM Preamplifier (Left channel) gain in 2 dB step	
			1	0	0	1	1	FM Preamplifier (Left channel) -20 dB gain	

*: state at power on initialization
X: reserved: write 0

Control Register CR11 Functions (Address: 0x0B)

7	6	5	4	3	2	1	0	Function
			FMRA(4:0)					
X	X	X						
			0	0	0	0	0	FM Preamplifier (Right channel) +18 dB gain
			0	0	0	0	1	FM Preamplifier (Right channel) +16 dB gain
			-	-	-	-	-	FM Preamplifier (Right channel) gain in 2 dB step
			0	1	0	0	1	FM Preamplifier (Right channel) 0 dB gain *
			-	-	-	-	-	FM Preamplifier (Right channel) gain in 2 dB step
			1	0	0	1	1	FM Preamplifier (Right channel) -20 dB gain

*: state at power on initialization
X: reserved: write 0

Control Register CR12 Functions (Address: 0x0C)

7	6	5	4	3	2	1	0	Function
TONEG(3:0)				FSEL(1:0)		SN	DE	
0	0	0	0					Tone gain is 0 dB *
0	0	0	1					Tone gain is -3 dB
-	-	-	-					Tone gain in 3 dB step
1	0	1	1					Tone gain is -33 dB
				0	0			f1 and f2 muted *
				0	1			f1 selected
				1	0			f2 selected
				1	1			f1 and f2 in summed mode
						0		Squarewave signal selected *
						1		Sinewave signal selected
							0	Tone/ Ring Generator not connected to Transmit path *
							1	Tone/ Ring Generator connected to Transmit path

*: state at power on initialization
X: reserved write 0

Control Register CR13 Functions (Address: 0x0D)

7	6	5	4	3	2	1	0	Function
F1(7:0)								
msb							lsb	Binary equivalent of the decimal number used to calculate f1 See Table 1

Control Register CR14 Functions (Address: 0x0E)

7	6	5	4	3	2	1	0	Function
F2(7:0)								
msb							lsb	Binary equivalent of the decimal number used to calculate f2 See Table 1

Control Register CR15 Functions (Address: 0x0F)

7	6	5	4	3	2	1	0	Function
BE	**BI**	**BZ(5:0)**						
0 1								Buzzer output disabled (set to 0) * Buzzer output enabled
	0 1							Duty Cycle is intended as the relative width of logic 1 * Duty cycle is intended as the relative width of logic 0
		msb					lsb	Binary equivalent of the decimal number used to calculate the duty cycle, using the formula: Duty Cycle = BZ(5:0) x 0.78125%

* state at power on initialization

Control Register CR16 Functions (Address: 0x10)

7	6	5	4	3	2	1	0	Function
POL	**ORD**	**DIF**	**INV**	**FOR**	**SCL**	**PREC(1:0)**		
0 1								AMCK Not Inverted * AMCK Inverted
	0 1							Audio I/F data order, the MSB is received first (I^2S) * Audio I/F data order, the LSB is received first
		0 1						Audio I/F data alignment, the word is left justified (I^2S)(1) * Audio I/F data alignment, the word is right justified (1)
			0 1					LRCK polarity, when LRCK=0 Left data is received (I^2S) (2) * LRCK polarity, when LRCK=1 Left data is received (2)
				0 1				Audio I/F format, I^2S format (first bit is delayed) (3) * Audio I/F format, non delayed formats
					0 1			SCK polarity, SDI and LRCK sampled on the rising edge (I^2S) * SCK polarity, SDI and LRCK sampled on the falling edge
						0 0 1 1	0 1 0 1	Audio I/F data width 16 bit (32 SCK clocks per frame) * Audio I/F data width 18 bit (64 SCK clocks per frame) Audio I/F data width 20 bit (64 SCK clocks per frame) Audio I/F data width 24 bit (64 SCK clocks per frame)

(1) significant in 18／ 20／ 24 bit per word mode only
(2) Left Channel data is always received first.
(3) First bit delay, in 18／ 20／ 24 bit per word mode, is applied only if word is left justified.
*: state at power on initialization

Control Register CR17 Functions (Address: 0x11)

7	6	5	4	3	2	1	0	Function
REN	RLM	ROI	RDL	OCE	SPIM	MSM	DSPM	
0 1								Remocon Function disabled * Remocon Function enabled
	0 1							Remocon output in transparent mode * Remocon output in latched mode
		0 1						REMOUT/OCK output not inverted * REMOUT/OCK output inverted
			0 1					Remocon detection latch reset by µP * Remocon detection latch set by internal logic
				0 1				REMOUT/OCK pin used for REMOCON function * REMOUT/OCK pin used for Oversampled Clock Out function (1)
					0 1			Audio interface works in I^2S or DSP mode * Audio interface works in SPI slave mode
						0 1		Audio interface works in Slave mode * Audio interface works in Master mode (1)
							0 1	Audio interface works in I^2S mode (1) * Audio interface works in DSP mode (1)

(1) significant if SPIM=0 (bit 2 in CR17)
*: state at power on initialization
X: reserved write 0

Control Register CR18 Functions (Address: 0x12)

7	6	5	4	3	2	1	0	Function
VCL		VCE				AMCK_DIV		
0 0 1 1	0 1 0 1							VCMHP output voltage is 1.20 V VCMHP output voltage is 1.35 V * VCMHP output voltage is 1.50 V VCMHP output voltage is 1.65 V
		0 1						VCMHP output Disabled * VCMHP output Enabled
			X	X	X			
						0 0 1	0 1 0	9.5MHz -14MHz AMCK clock-range * 14MHz -19MHz AMCK clock-range 19MHz -28MHz AMCK clock-range

*: state at power on initialization
X: reserved write 0

Control Register CR19 Functions (Address: 0x13)

7	6	5	4	3	2	1	0	Function
	TREBLE(2:0)			BASS(3:0)				
X								
	0	1	1					+6dB Treble Gain
	0	1	0					+4dB Treble Gain
	0	0	1					+2dB Treble Gain
	0	0	0					0dB Treble Gain *
	1	1	1					-2dB Treble Gain
	1	1	0					-4dB Treble Gain
	1	0	1					-6dB Treble Gain
	1	0	0					De-emphasis filter enabled
				0	1	0	1	+12.5dB Bass Gain
				0	1	0	0	+10.0dB Bass Gain
				0	0	1	1	+7.5dB Bass Gain
				0	0	1	0	+5.0dB Bass Gain
				0	0	0	1	+2.5dB Bass Gain
				0	0	0	0	0dB Bass Gain *
				1	1	1	1	-2.5dB Bass Gain
				1	1	1	0	-5.0dB Bass Gain
				1	1	0	1	-7.5dB Bass Gain
				1	1	0	0	-10.0dB Bass Gain
				1	0	1	1	-12.5dB Bass Gain

*: state at power on initialization
X: reserved write 0

Control Register CR20 Functions (Address: 0x14)

7	6	5	4	3	2	1	0	Function
FMS	MFM	CMP	VOL (4:0)					
0								FM sum function disabled *
1								FM sum function enabled
	0							FM input from FML, FMR *
	1							FM input from MIC3 (to Left and Right)
		0						Audio Dynamic compressor OFF *
		1						Audio Dynamic compressor ON
			0	0	0	0	0	0 dB Audio Attenuation *
			0	0	0	0	1	2 dB Audio Attenuation
			0	0	0	1	0	4 dB Audio Attenuation
			0	0	0	1	1	6 dB Audio Attenuation
			0	0	1	0	0	8 dB Audio Attenuation
			0	0	1	0	1	10 dB Audio Attenuation
			0	0	1	1	0	12 dB Audio Attenuation
			0	0	1	1	1	15 dB Audio Attenuation
			0	1	0	0	0	18 dB Audio Attenuation
			0	1	0	0	1	21 dB Audio Attenuation
			0	1	0	1	0	24 dB Audio Attenuation
			0	1	0	1	1	27 dB Audio Attenuation
			0	1	1	0	0	30 dB Audio Attenuation
			0	1	1	0	1	33 dB Audio Attenuation
			0	1	1	1	0	36 dB Audio Attenuation
			0	1	1	1	1	39 dB Audio Attenuation
			1	0	0	0	0	42 dB Audio Attenuation
			1	0	0	0	1	45 dB Audio Attenuation
			1	0	0	1	0	48 dB Audio Attenuation
			1	0	0	1	1	54 dB Audio Attenuation

*: state at power on initialization

Control Register CR21 Functions (Address: 0x15)

7	6	5	4	3	2	1	0	Function
MD(1:0)		CFM(1:0)				SRS	PU	
0 0 1 1	0 1 0 1							Voice Mode * Audio Mode. Tone Only Mode. FM Mode.
		0 0 1	0 1 X					The Master Clock Input for Tone Only and FM Mode is AUXCLK* The Master Clock Input for Tone Only and FM Mode is MCLK The Master Clock Input for Tone Only and FM Mode is AMCK
				X	X			
						0 1		Normal Operation * Software Reset, all registers are set to their default.
							0 1	Device is in Power Down * Device is in Power Up

*: state at power on initialization

X: reserved write 0

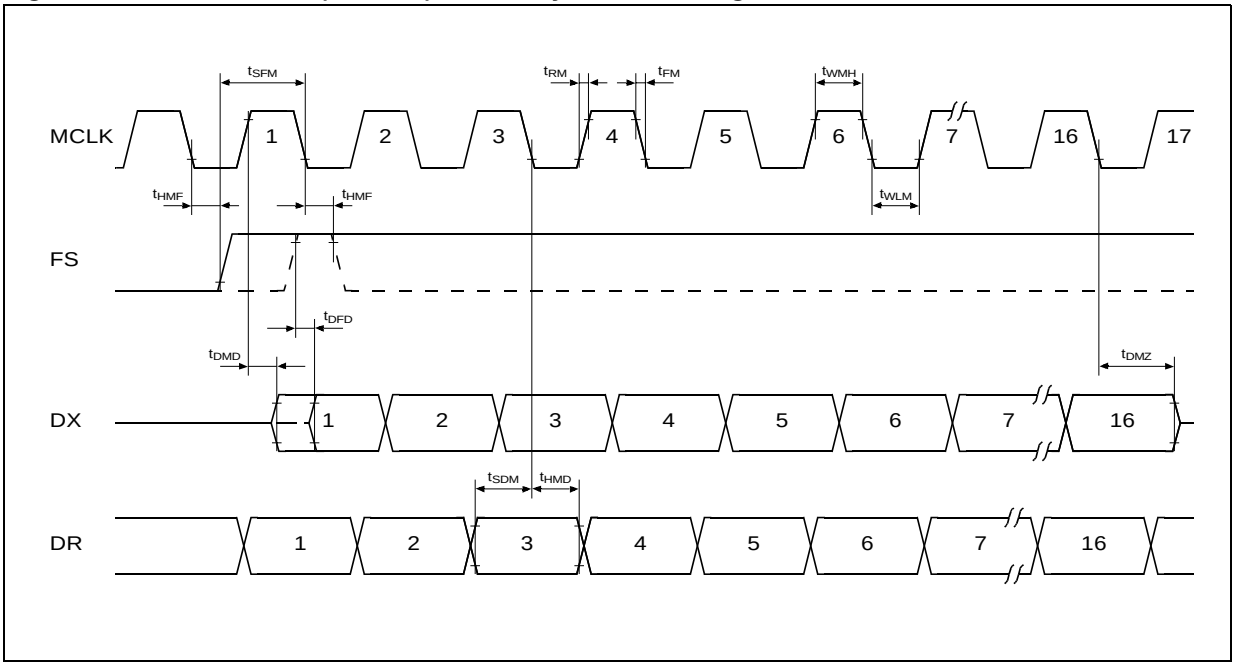
Note: In Audio mode or when **AMCK** Master Clock is selected, the true frequency value is obtained by multiplying the value of the table (F1/F2 Tone Frequency) by the following constant: $k=(f_{AMCK}/f_{DIV})$ where f_{AMCK} is the frequency of **AMCK** expressed in Hz and $f_{DIV}=6144000\cdot(AMCK\_DIV+2)$, where AMCK_DIV is the content of **CR18**, bits1-0.

Table 1. Tone generator frequency versus CR13 CR14 register correspondence in voice mode and tone mode only (when the master clock is AUXCLK or MCLK)

CR13/14 Value (dec.)	F1/F2 Tone Frequency (Hz)	CR13/14 Value (dec.)	F1/F2 Tone Frequency (Hz)	CR13/14 Value (dec.)	F1/F2 Tone Frequency (Hz)	CR13/14 Value (dec.)	F1/F2 Tone Frequency (Hz)
0	0.0	64	250.0	128	750.0	192	1750.0
1	3.9	65	257.8	129	765.6	193	1781.2
2	7.8	66	265.6	130	781.2	194	1812.5
3	11.7	67	273.4	131	796.9	195	1843.8
4	15.6	68	281.2	132	812.5	196	1875.0
5	19.5	69	289.1	133	828.1	197	1906.2
6	23.4	70	296.9	134	843.8	198	1937.5
7	27.3	71	304.7	135	859.4	199	1968.8
8	31.2	72	312.5	136	875.0	200	2000.0
9	35.2	73	320.3	137	890.6	201	2031.2
10	39.1	74	328.1	138	906.2	202	2062.5
11	43.0	75	335.9	139	921.9	203	2093.8
12	46.9	76	343.8	140	937.5	204	2125.0
13	50.8	77	351.6	141	953.1	205	2156.2
14	54.7	78	359.4	142	968.8	206	2187.5
15	58.6	79	367.2	143	984.4	207	2218.8
16	62.5	80	375.0	144	1000.0	208	2250.0
17	66.4	81	382.8	145	1015.6	209	2281.2
18	70.3	82	390.6	146	1031.2	210	2312.5
19	74.2	83	398.4	147	1046.9	211	2343.8
20	78.1	84	406.2	148	1062.5	212	2375.0
21	82.0	85	414.1	149	1078.1	213	2406.2
22	85.9	86	421.9	150	1093.8	214	2437.5
23	89.8	87	429.7	151	1109.4	215	2468.8
24	93.8	88	437.5	152	1125.0	216	2500.0
25	97.7	89	445.3	153	1140.6	217	2531.2
26	101.6	90	453.1	154	1156.2	218	2562.5
27	105.5	91	460.9	155	1171.9	219	2593.8
28	109.4	92	468.8	156	1187.5	220	2625.0
29	113.3	93	476.6	157	1203.1	221	2656.2
30	117.2	94	484.4	158	1218.8	222	2687.5
31	121.1	95	492.2	159	1234.4	223	2718.8
32	125.0	96	500.0	160	1250.0	224	2750.0
33	128.9	97	507.8	161	1265.6	225	2781.2
34	132.8	98	515.6	162	1281.2	226	2812.5
35	136.7	99	523.4	163	1296.9	227	2843.8
36	140.6	100	531.2	164	1312.5	228	2875.0
37	144.5	101	539.1	165	1328.1	229	2906.2
38	148.4	102	546.9	166	1343.8	230	2937.5
39	152.3	103	554.7	167	1359.4	231	2968.8
40	156.2	104	562.5	168	1375.0	232	3000.0
41	160.2	105	570.3	169	1390.6	233	3031.2
42	164.1	106	578.1	170	1406.2	234	3062.5
43	168.0	107	585.9	171	1421.9	235	3093.8
44	171.9	108	593.8	172	1437.5	236	3125.0
45	175.8	109	601.6	173	1453.1	237	3156.2
46	179.7	110	609.4	174	1468.8	238	3187.5
47	183.6	111	617.2	175	1484.4	239	3218.8
48	187.5	112	625.0	176	1500.0	240	3250.0
49	191.4	113	632.8	177	1515.6	241	3281.2
50	195.3	114	640.6	178	1531.2	242	3312.5
51	199.2	115	648.4	179	1546.9	243	3343.8
52	203.1	116	656.2	180	1562.5	244	3375.0
53	207.0	117	664.1	181	1578.1	245	3406.2
54	210.9	118	671.9	182	1593.8	246	3437.5
55	214.8	119	679.7	183	1609.4	247	3468.8
56	218.8	120	687.5	184	1625.0	248	3500.0
57	222.7	121	695.3	185	1640.6	249	3531.2
58	226.6	122	703.1	186	1656.2	250	3562.5
59	230.5	123	710.9	187	1671.9	251	3593.8
60	234.4	124	718.8	188	1687.5	252	3625.0
61	238.3	125	726.6	189	1703.1	253	3656.2
62	242.2	126	734.4	190	1718.8	254	3687.5
63	246.1	127	742.2	191	1734.4	255	3718.8

TIMING DIAGRAMS

Figure 1. Voice interface (PCM I/F) non delayed data timing mode[1]



Note: 1. In the case of companded code the timing is applied to 8 bits instead of 16 bits.

Figure 2. Voice interface (PCM I/F) delayed data timing mode[1]

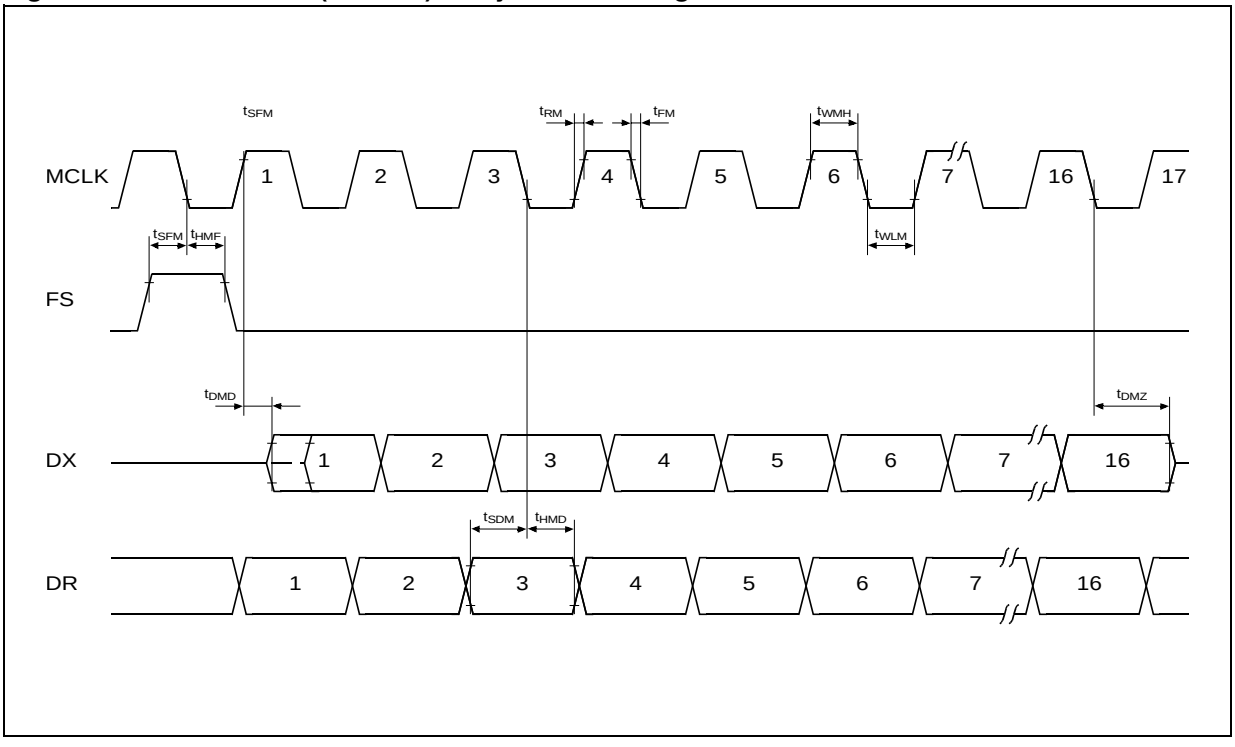
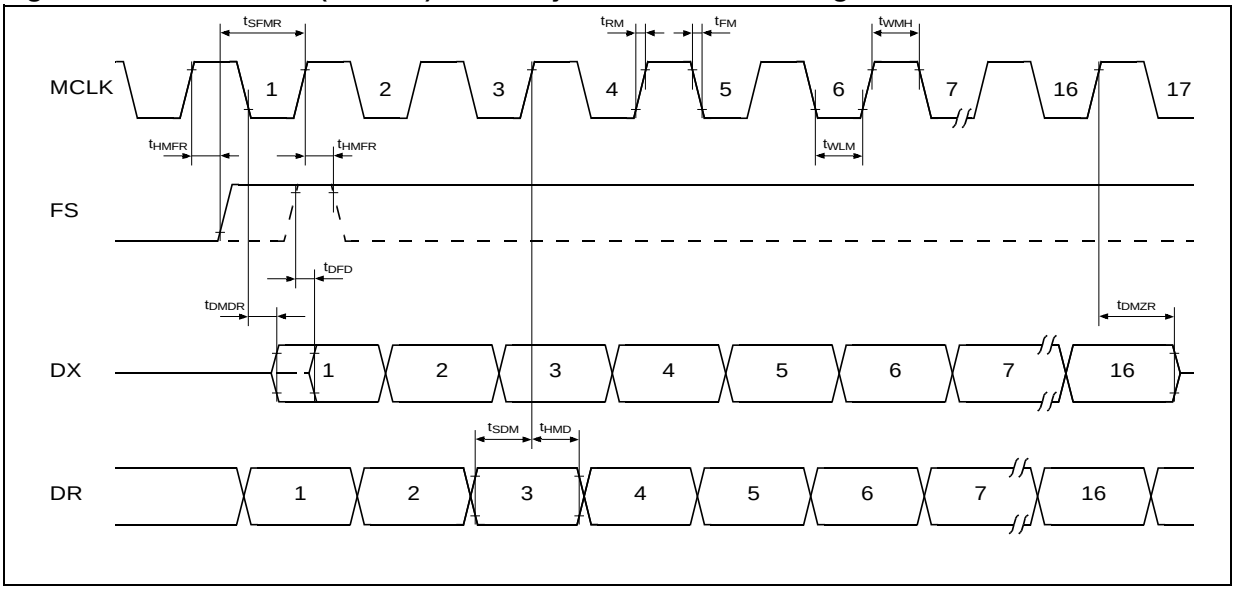


Figure 3. Voice interface (PCM I/F) non delayed reverse data timing mode [1]



Note: 1. In the case of companded code the timing is applied to 8 bits instead of 16 bits.

Figure 4. AMCK timing

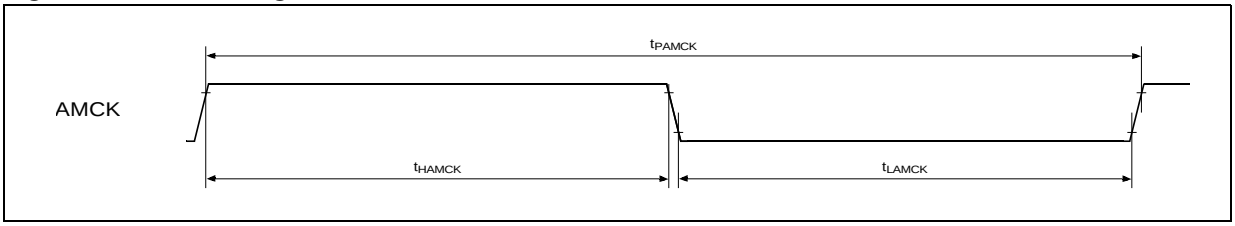
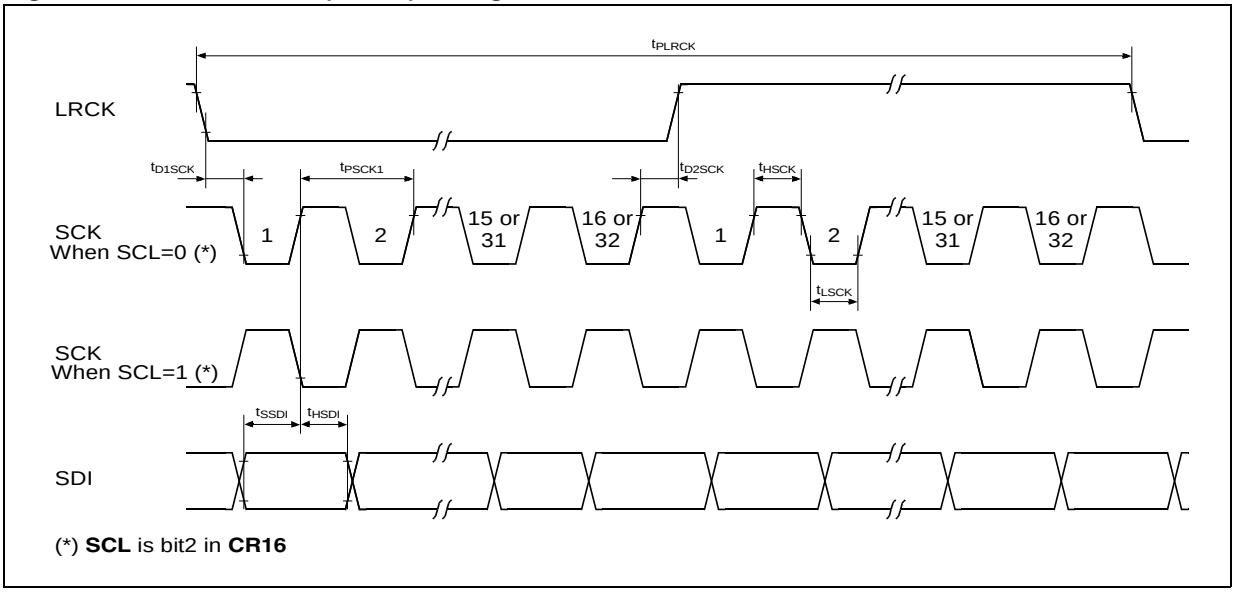
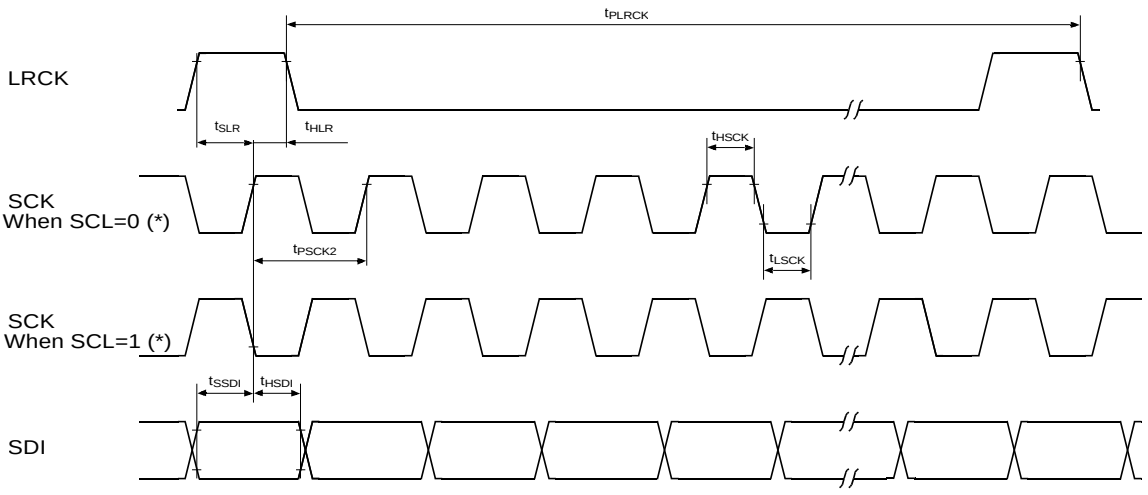


Figure 5. Audio interface (AU I/F) timing: I²S slave mode



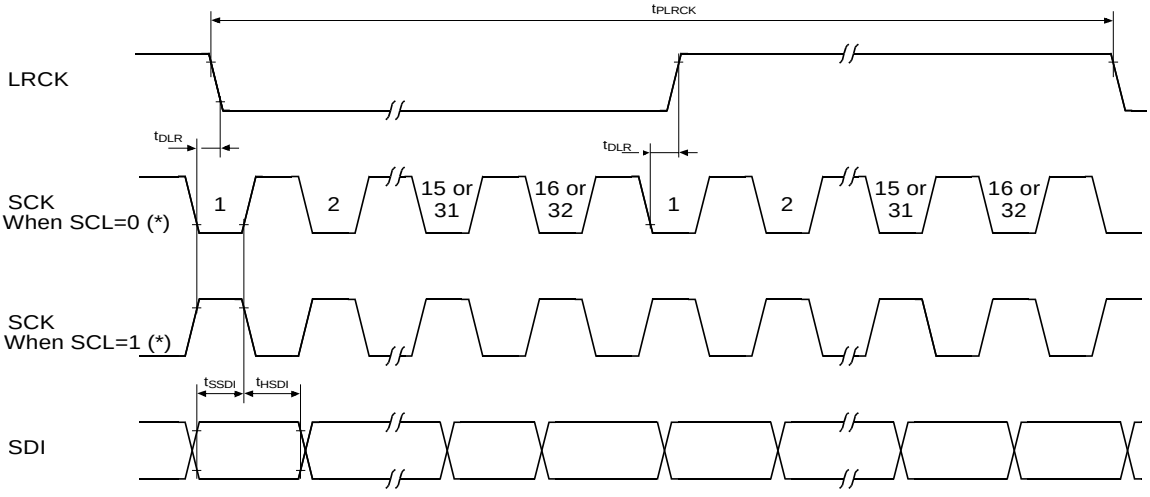
(*) **SCL** is bit2 in **CR16**

Figure 6. Audio interface (AU I/F) timing: DSP slave mode



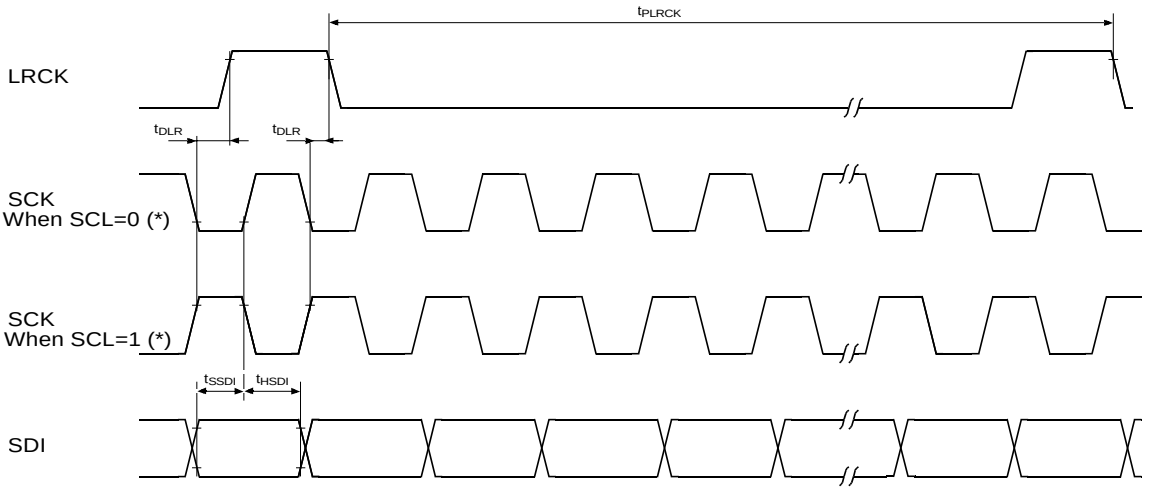
(*) **SCL** is bit2 in **CR16**

Figure 7. Audio interface (AU I/F) timing: I^2S master mode



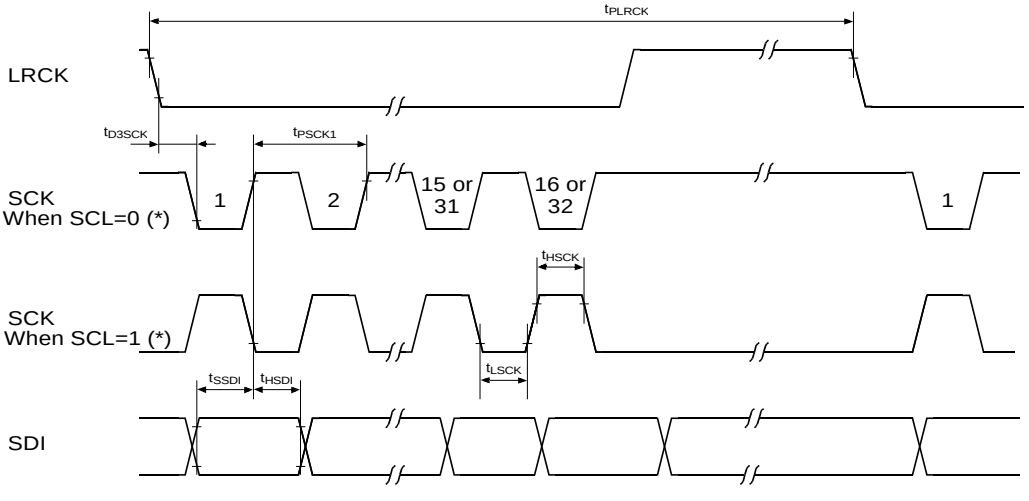
(*) **SCL** is bit2 in **CR16**

Figure 8. Audio interface (AU I/F) timing: DSP master mode



(*) **SCL** is bit2 in **CR16**

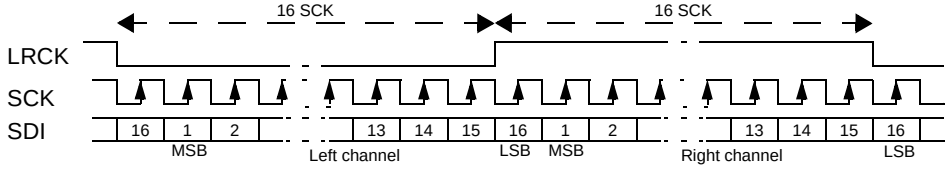
Figure 9. Audio interface (AU I/F) timing: SPI-mode (slave only)



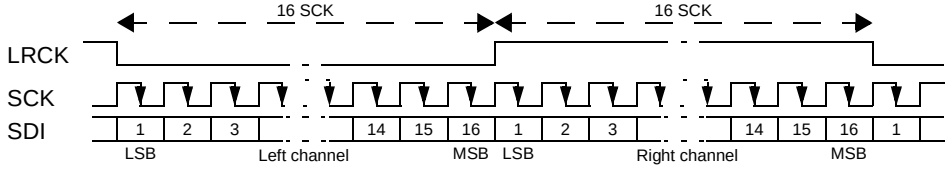
(*) **SCL** is bit2 in **CR16**

Figure 10. Audio interface (AU I/F) formats in I^2S master and slave modes

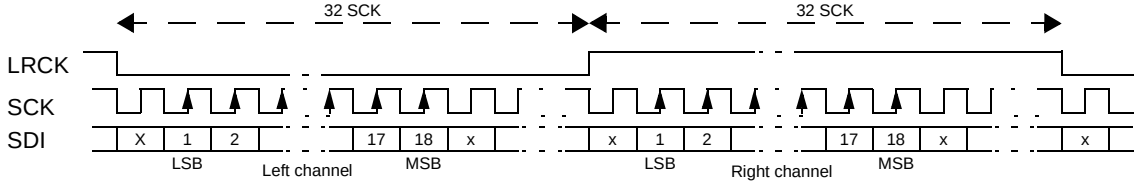
I^2S Format (delayed), Data word 16 bit, MSB first (default)



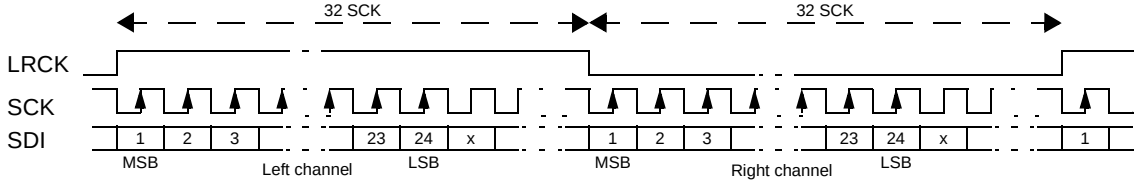
Non-delayed Format, SCK polarity inverted, Data word 16 bit, LSB first



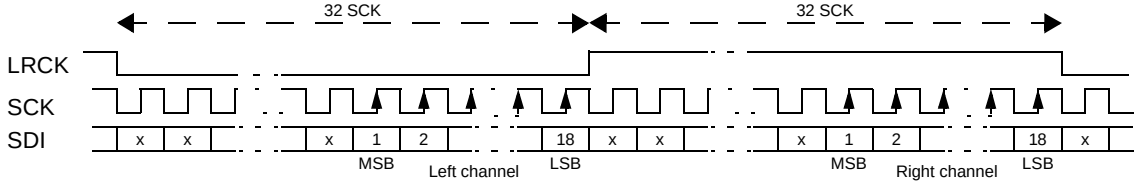
I^2S Format (delayed), Data word 18 bit, Left justified, LSB first



Non-delayed Format, Data word 24 bit, Left justified, MSB first, LRCK polarity inverted



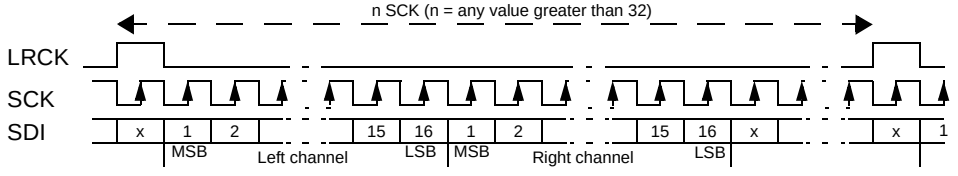
Data word 18 bit, Right justified, MSB first



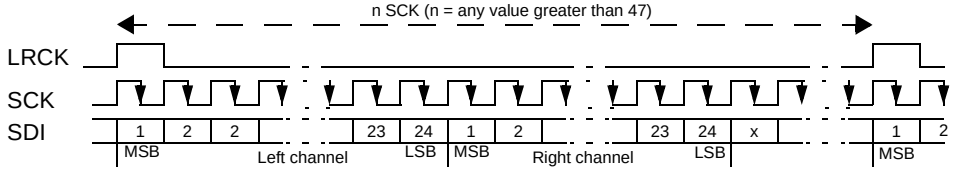
For the other possible formats see Control Register **CR16** description

Figure 11. Audio interface (AU I/F) formats in DSP slave mode

Delayed, Data word 16 bit, SCK polarity normal (**CR16** default values)



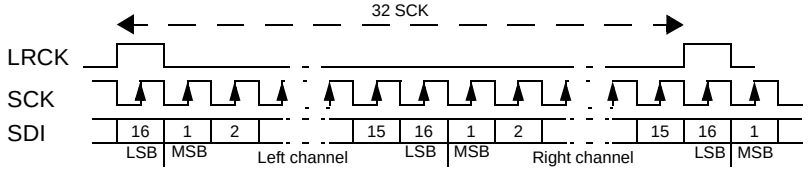
Non-delayed, SCK polarity inverted, Data word 24 bit



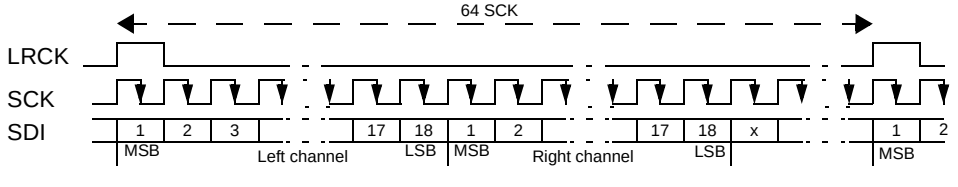
For the other possible formats see Control Register **CR16** description

Figure 12. Audio interface (AU I/F) formats in DSP master mode

Delayed, Data word 16 bit, SCK polarity normal (**CR16** default values)



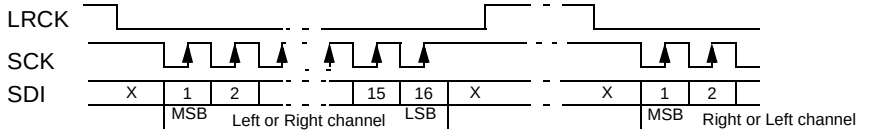
Non-delayed, SCK polarity inverted, Data word 18 bit



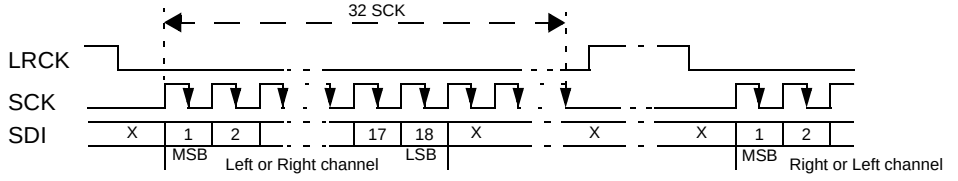
For the other possible formats see Control Register **CR16** description

Figure 13. Audio interface (AU I/F) formats in SPI mode

SCK polarity normal, Data word 16 bit



SCK polarity inverted, Data word 18 bit



NOTE: In SPI-mode the first high to low transition on LRCK after power-up defines the Left channel of the first couple of audio data and of all the subsequent couples of Left/Right audio data.

For the other possible formats see Control Register **CR16** description

Figure 14. Control interface (I^2C I/F) formats

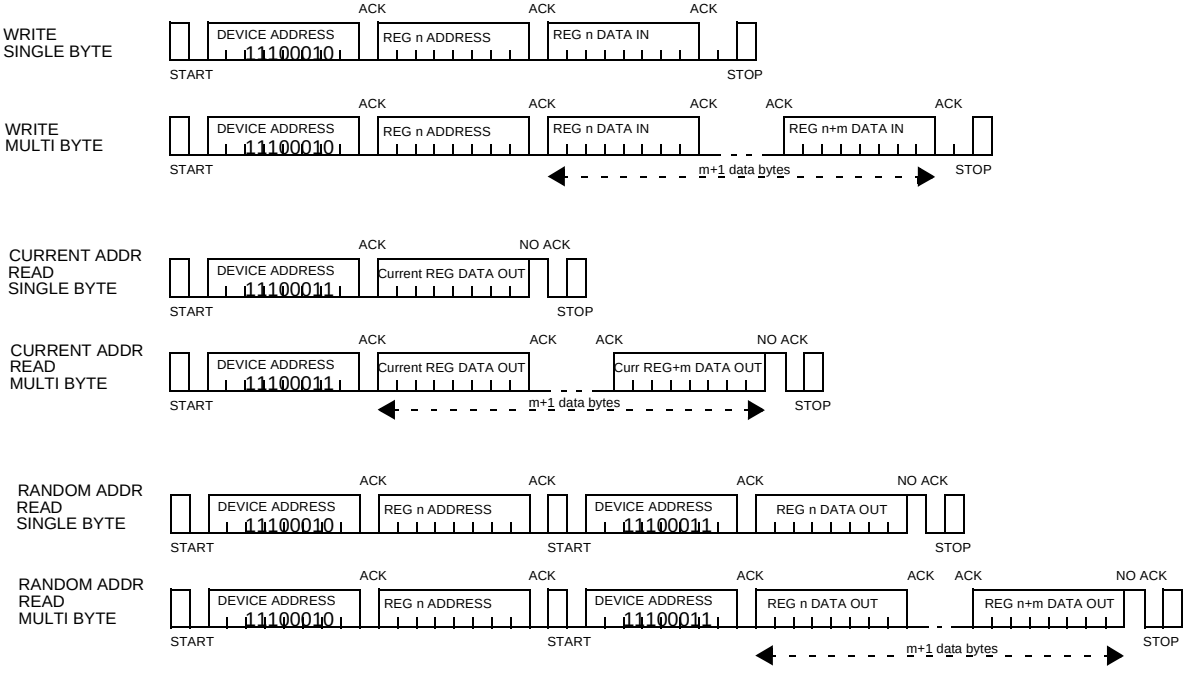


Figure 15. Control interface (I^2C I/F) timing

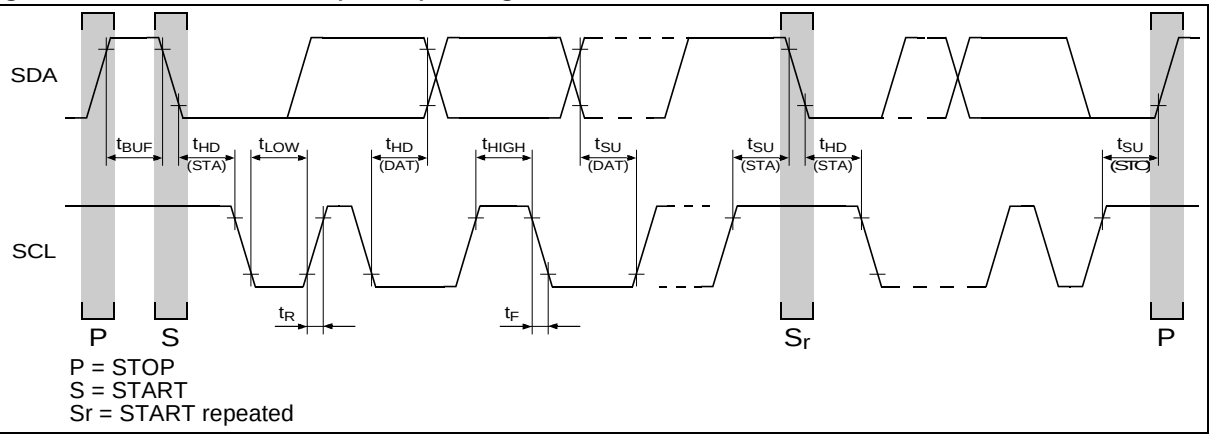
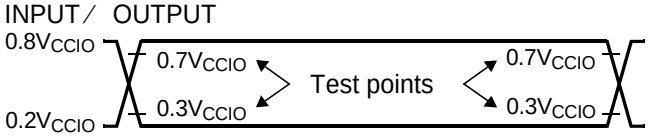


Figure 16. A.C. Testing input, output waveform



AC Testing: inputs are driven at 0.8VCCIO for a logic "1" and 0.2VCCIO for a logic "0".
Timing measurements are made at 0.7VCCIO for a logic "1" and 0.3VCCIO for a logic "0".

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
V_{CC} to GND	4.6	V
Voltage at MIC (V_{CC} ≤3.3V)	V_{CC} +0.5 to GND -0.5	V
Current at LSP/N	± 350	mA
Current at HPR,HPL	± 100	mA
Current at VCCP,GNDP	± 350	mA
Current at any digital output	± 50	mA
Voltage at any digital input (V_{CCIO} ≤3.3V); limited at ± 50mA	V_{CCIO} + 0.5 to GND -0.5	V
Storage temperature range	- 65 to + 150	°C

OPERATIVE SUPPLY VOLTAGES

Symbol	Min.	Max.	Unit
$V_{CC} = V_{CCA}$	2.7	3.3	V
V_{CCIO}	1.8	V_{CC}	V
V_{CCP}	V_{CC}	3.3	V

TIMING SPECIFICATIONS

Unless otherwise specified, V_{CCIO} = 1.8V to 3.3V,T_{amb} = -30°C to 85°C, max capacitive load 20pF; typical characteristics are specified at V_{CCIO} = 3.0V, T_{amb} = 25 °C; all signals are referenced to GND (see next Note for timing definitions).

AMCK timing

Symbol	Parameter	Test Condition	AMCK Range	Min.	Typ.	Max.	Unit
t_{PAMCK}	Period of AMCK		9.5MHz-14MHz 14MHz-19MHz 19MHz-28MHz	71 53 36		106 71 53	ns ns ns
t_{HAMCK}	Period of AMCK high	Measured from V_{IH} to V_{IH}	9.5MHz-14MHz 14MHz-19MHz 19MHz-28MHz	28 20 12			ns ns ns
t_{LAMCK}	Period of AMCK low	Measured from V_{IL} to V_{IL}	9.5MHz-14MHz 14MHz-19MHz 19MHz-28MHz	28 20 12			ns ns ns

MCLK and AUXCLK timing

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{MCLK}	Frequency of MCLK, AUXCLK	Frequency is programmable with bits **F** in **CR0**		512 1.536 2.048 2.560		kHz MHz MHz MHz
t_{WMH}	Period of MCLK, AUXCLK high	Measured from V_{IH} to V_{IH}	150			ns
t_{WML}	Period of MCLK, AUXCLK low	Measured from V_{IL} to V_{IL}	150			ns
t_{RM}	Rise Time of MCLK, AUXCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK, AUXCLK	Measured from V_{IH} to V_{IL}			30	ns

Audio interface signals timing

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{PLRCK}	Period of LRCK		20		127	µs
DC_{LRCK}	Duty Cycle of LRCK in I^2S mode Slave		40		60	%
t_{D1SCK}	Delay of the 1st SCK edge from LRCK edges in I^2S mode Slave		-10		600	ns
t_{D2SCK}	Delay of the last SCK edge to next LRCK edges in I^2S mode Slave		20			ns
t_{PSCK1}	Period of SCK in I^2S mode Slave		50			ns
t_{PSCK2}	Period of SCK in DSP mode Slave	LRCK frequency > 30kHz LRCK frequency < 30kHz	100 200			ns ns
t_{HSCK}	Period of SCK high	Measured from V_{IH} to V_{IH}	20			ns
t_{LSCK}	Period of SCK low	Measured from V_{IL} to V_{IL}	20			ns
t_{SSDI}	Setup time SDI to SCK active edge		10			ns
t_{HSDI}	Hold time SDI from SCK active edge		10			ns
t_{DLR}	Delay of LRCK edges from SCK edge in Master mode				10	ns
t_{D3SCK}	Delay of the 1st SCK edge from LRCK falling edge in SPI mode		-10			ns

PCM interface timing

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{HMF}	Hold Time MCLK low to FS low		0			ns
t_{SFM}	Setup Time, FS high to MCLK low		30			ns
t_{DMD}	Delay Time, MCLK high to data valid	Load = 20pF			100	ns
t_{DMZ}	Delay Time, MCLK low to DX disabled		10		100	ns
t_{DFD}	Delay Time, FS high to data valid	Load = 20pF; Applies only if FS rises later than MCLK rising edge in Non Delayed Mode only			100	ns
t_{SDM}	Setup Time, DR valid to MCLK receive edge		20			ns

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{HMD}	Hold Time, MCLK low to DR invalid		10			ns
t_{HMFR}	Hold Time MCLK High to FS low		30			ns
t_{SFMR}	Setup Time, FS high to MCLK High		30			ns
t_{DMDR}	Delay Time, MCLK low to data valid	Load = 20pF			100	ns
t_{DMZR}	Delay Time, MCLK High to DX disabled		10		100	ns
t_{HMDR}	Hold Time, MCLK High to DR invalid		20			ns

I^2C bus control port timing

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Clock Frequency				400	kHz
t_{HIGH}	Clock High Time		600			ns
t_{LOW}	Clock Low Time		1300			ns
t_R	SDA and SCL Rise Time				1000	ns
t_F	SDA and SCL Fall Time				300	ns
$t_{HD:STA}$	Start Condition Hold Time		600			ns
$t_{SU:STA}$	Start Condition Setup Time		600			ns
$t_{HD:DAT}$	Data Input Hold Time		0			ns
$t_{SU:DAT}$	Data Input Setup Time		250			ns
$t_{SU:STO}$	Stop Condition Setup Time		600			ns
t_{BUF}	Bus Free Time		1300			ns

Note: A signal is valid if it is above VIH or below VIL and invalid if it is between VIL and VIH.For the purpose of this specification the following conditions apply (see Fig. 15):

a) All input signal are defined as: VIL = 0.2VCCIO, VIH = 0.8VCCIO, tR < 10ns, tF < 10ns.

b) Delay times are measured from the inputs signal valid to the output signal valid.

c) Setup times are measured from the data input valid to the clock input invalid.

d) Hold times are measured from the clock signal valid to the data input invalid.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CCIO} = 1.8V to 3.3V, T_{amb} = -30°C to 85°C; typical characteristic are specified at V_{CCIO} = 3.0V, T_{amb} = 25°C; all signals are referenced to GND.

Digital Interfaces (Figure 16)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All digital inputs except REMIN REMIN	DC AC			$0.3V_{CCIO}$ $0.2V_{CCIO}$	V V
V_{IH}	Input High Voltage	All digital inputs except REMIN REMIN	DC AC	0.7_{VCCIO} 0.8_{VCCIO}			V V
V_{ILREM}	Input Low Voltage	REMIN input				0.5	V
V_{IHREM}	Input High Voltage	REMIN input		1.4			V
V_{OL}	Output Low Voltage	All digital outputs, I_L = 10µA All digital outputs, I_L = 2mA				0.1 0.4	V V
V_{OH}	Output High Voltage	All digital outputs, IL = 10µA All digital outputs, IL = 2mA		V_{CCIO}-0.1 V_{CCIO}-0.4			V V
I_{IL}	Input Low Current	Any digital input, GND < V_{IN} < V_{IL}		-10		10	µA
I_{IH}	Input High Current	Any digital input, V_{IH} < V_{IN} < V_{CCIO}		-10		10	µA
I_{OZ}	Output Current in High impedance (Tristate)	DX and CO		-10		10	µA

Analog Interfaces

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{MBIAS}	MBIAS Output Resistance	MBIAS 100mV under V_{CC}			150	Ω
I_{MIC}	MIC Input Leakage	GND < V_{MIC} < V_{CC}	-100		+100	µA
R_{MIC}	MIC Input Resistance	GND < V_{MIC} < V_{CC}	50			kΩ
R_{FM}	FM Input Resistance	FML, FMR to CAP2	30			kΩ
R_{LHP}	Single Ended Drivers Load Resistance	HPL, HPR to GNDP or VCMHP	16			Ω
C_{LHP}	Single Ended Drivers Load Capacitance	HPL, HPR to GNDP or VCMHP		100 50*		pF nF
R_{OVHP}	Single Ended Drivers Output Resistance	Steady zero PCM code applied to DR; I = ±1mA		1		Ω
R_{LLS}	Differential Driver Load Resistance	LSP to LSN	8			Ω
C_{LLS}	Differential Driver Load Capacitance	LSP to LSN		100 50*		pF nF
R_{OLS}	Differential Driver Output Resistance	Steady zero PCM code applied to DR; I = ±1mA		1		Ω
V_{OSLS}	Differential offset Voltage at LSP, LSN	Alternating ± zero PCM code applied to DR maximum receive gain; R_L = 50Ω	-50		+50	mV

*: with series resistors

ANALOG INPUT/OUTPUT OPERATIVE RANGES

Microphone Input Levels - Absolute levels at MIC1, MIC2, MIC3

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	0 dBm0 level	Transmit gain 0dB		493		mV_{RMS}
	Overload level	Transmit gain 0dB		707 2		mV_{RMS} V_{pp}
	0 dBm0 level	Transmit gain 20dB		49		mV_{RMS}
	Overload level	Transmit gain 20dB		71 200		mV_{RMS} mV_{pp}
	0 dBm0 level	Transmit gain 42.5dB		3.7		mV_{RMS}
	Overload level	Transmit gain 42.5dB		5.3 15		mV_{RMS} mV_{pp}

FM Input Levels - Absolute levels at FML, FMR

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Overload level	FML, FMR gain 18 dB		177 0.5		mV_{RMS} V_{pp}
	Overload level	FML, FMR gain from 6 to -20dB		707 2		mV_{RMS} V_{pp}

Power Output Levels - Absolute levels at HPL, HPR

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Maximum undistorted level	16Ω Load	707 2			mV_{RMS} V_{pp}

Power Output Levels - Absolute levels at LSP-LSN (Differentially measured)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	0 dBm0 level	LS gain 0dB		984		mV_{RMS}
	0 dBm0 level	LS gain -24dB		62.1		mV_{RMS}
	Maximum undistorted level	8Ω Load	1.41 4			V_{RMS} V_{pp}

Tones Levels

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Tone level at LSP-LSN	Single tone, sinusoidal waveform, tone gain 0dB, LS gain 0dB		1.41 4		V_{RMS} V_{pp}
	Tone level at HPL, HPR	Single tone, sinusoidal waveform, tone gain 0dB, HPL, HPR gain -6dB		707 2		mV_{RMS} V_{pp}
	Tone level at DX	Voice mode, Single tone, sinusoidal waveform, tone gain 0dB		-1.64		dBFS

Note: when 2 tones are enabled the amplitude of f1 is lowered by 5dB and the amplitude of f2 is lowered by 7dB with respect to the amplitude of a single tone.

VOICE CODEC CHARACTERISTICS

Unless otherwise specified, V_{CC} = 2.7V to 3.3V, T_{amb} = -30°C to 85°C; FS Frequency = 8kHz; typical characteristics are specified at V_{CC} = 3.0V, T_{amb} = 25°C, MIC1／ 2／ 3 = 0dBm0, DR = -6dBm0 PCM code, f = 1015.625 Hz; all signals are referenced to GND.

VOICE CODEC AMPLITUDE RESPONSE

Transmit path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for minimum. Measure deviation of Digital PCM Code from ideal $0dB_{m0}$ PCM code at DX	-0.5		0.5	dB
G_{XAG}	Transmit Gain Variation with programmed gain	Measure Transmit Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GXA, i.e. $G_{AXG} = G_{actual} - G_{prog.} - G_{XA}$	-0.5		0.5	dB
G_{XAT}	Transmit Gain Variation with temperature	Measured relative to G_{XA}. min. gain < G_X < Max. gain	-0.1		0.1	dB
G_{XAV}	Transmit Gain Variation with supply	Measured relative to G_{XA} G_X = Minimum gain	-0.1		0.1	dB
G_{XAF8}	Transmit Gain Variation with frequency. FS Frequency = 8kHz (VFS=0)	Digital filter characteristics f = 60 Hz f = 100 Hz f = 200 Hz f = 300 Hz f = 400 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz (*) f = 8000 Hz (*)	 -1.5 -0.5 -1.5		 -30 -20 -6 0.5 0.5 0.0 -14 -35 -47	 dB dB dB dB dB dB dB dB dB
G_{XAF16}	Transmit Gain Variation with frequency. FS Frequency = 16kHz (VFS=1)	Digital filter characteristics f = 100 Hz f = 200 Hz to 6000 Hz f = 6800 Hz f = 8000 Hz f = 9200 Hz (*) f = 16000 Hz (*)	 -1.5 -0.5 -1.5		 0.5 0.5 0.0 -14 -35 -47	 dB dB dB dB dB dB
G_{XAL}	Transmit Gain Variation with signal level	Sinusoidal Test method. Reference Level = -10 dBm0 V_{MIC} = -40 dBm0 to +3 dBm0 V_{MIC} = -50 dBm0 to -40 dBm0 V_{MIC} = -55 dBm0 to -50 dBm0	 -0.5 -0.5 -1.2		 0.5 0.5 1.2	 dB dB dB

(*) The limit at frequencies between 4600Hz and 8000Hz lies on a straight line connecting the two frequencies on a linear (dB) scale versus log (Hz) scale.

VOICE CODEC AMPLITUDE RESPONSE (continued)

Receive path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{RAHPL} G_{RAHPR} G_{RALS}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply -6 dBm0 PCM code to DR Measure HPL, HPR, LSP-LSN	-0.5		0.5	dB
G_{RAGHPL} G_{RAGHPR} G_{RAGLS}	Receive Gain Variation with programmed gain	Measure HPL, HPR, LSP-LSN Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to G_{RA}, i.e. $G_{RAGLS} = G_{actual} - G_{prog.} - G_{RALS}$	-0.5		0.5	dB
G_{RAT}	Receive Gain Variation with temperature	Measured relative to GRA. (HPL, HPR and LSP-LSN) min. gain < G_R < Max. gain	-0.1		0.1	dB
G_{RAV}	Receive Gain Variation with Supply	Measured relative to GRA. (HPL, HPR and LSP-LSN) G_R = Maximum Gain	-0.1		0.1	dB
G_{RAF8}	Receive Gain Variation with frequency (HPL, HPR and LSP-LSN) FS frequency = 8kHz (VFS=0). High Pass Filter enabled (HPB = 0).	Digital filter characteristics f = 60Hz f = 100Hz f = 200 Hz f = 300 Hz f = 400 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz	 -1.5 -0.5 -1.5		 -20 -12 -2 0.5 0.5 0.0 -14	 dB dB dB dB dB dB dB
	Receive Gain Variation with frequency (HPL, HPR and LSP-LSN) FS frequency = 8kHz (VFS=0). High Pass Filter disabled (HPB = 1).	Digital filter characteristics f = 50Hz f = 100 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz	 -1.5 -0.5 -1.5		 0.5 0.5 0.0 -14	 dB dB dB dB
G_{RAF16}	Receive Gain Variation with frequency (HPL, HPR and LSP-LSN) FS frequency = 16kHz (VFS=1).	Digital filter characteristics f = 100Hz f = 200 Hz to 6000 Hz f = 6800 Hz f = 8000 Hz	 -1.5 -0.5 -1.5		 0.5 0.5 0.0 -14	 dB dB dB dB
G_{RALHPL} G_{RALHPR} G_{RALLS}	Receive Gain Variation with signal level (HPL, HPR and LSP-LSN)	Sinusoidal Test Method Reference Level = -10 dBm0 DR = -40 dBm0 to -3 dBm0 DR = -50 dBm0 to -40 dBm0 DR = -55 dBm0 to -50 dBm0	 -0.5 -0.5 -1.2		 0.5 0.5 1.2	 dB dB dB

VOICE CODEC ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DXA	Tx Delay, Absolute	f = 1600 Hz		320		µs
DXR	Tx Delay, Relative	f = 500 - 600 Hz f = 600 - 800 Hz f = 800 - 1000 Hz f = 1000 - 1600 Hz f = 1600 - 2600 Hz f = 2600 - 2800 Hz f = 2800 - 3000 Hz		290 180 50 20 55 80 180		µs µs µs µs µs µs µs
DRA	Rx Delay, Absolute	f = 1600 Hz		280		µs
DRR	Rx Delay, Relative	f = 500 - 600 Hz f = 600 - 800 Hz f = 800 - 1000 Hz f = 1000 - 1600 Hz f = 1600 - 2600 Hz f = 2600 - 2800 Hz f = 2800 - 3000 Hz		200 110 50 20 65 100 220		µs µs µs µs µs µs µs

VOICE CODEC NOISE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NXP	Tx Noise, P weighted (up to 35dB)	V_{MIC} = 0V, DE = 0		-75	-70	dBm0p
NRP	Rx Noise, C-message weighted 8Ω Load (gain for max. undistorted output level)	Receive PCM code = Zero, SI = 0, RTE = 0 and LSA='0100' (gain -2dB)		30	50	μV_{RMS}
PSRTX	PSRR, Tx	MIC = 0V, V_{CC} = 3.0 V_{DC} + 50 mV_{RMS}; f = 100Hz to 50kHz	 30			 dB
PSRRX	PSRR, Rx	PCM Code equals Positive Zero, V_{CC} = 3.0V_{DC} + 50 mV_{RMS} f = 100 Hz - 4 kHz f = 4 kHz - 50 kHz	 30 30			 dB dB
SOS	Spurious Out-Band signal at the output	Digital filter characteristics 4600 Hz - 5600 Hz 5600 Hz - 7600 Hz 7600 Hz - 8400 Hz			 -40 -50 -50	 dB dB dB

(*) 300 to 3400Hz bandwidth

VOICE CODEC CROSSTALK

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive	Transmit Level = 0 dBm0, f = 300 - 3400 Hz DR = Quiet PCM Code		-100	-65	dB
CT_{R-X}	Receive to Transmit	Receive Level = -6 dBm0, f = 300 - 3400 Hz MIC = 0V		-80	-65	dB

VOICE CODEC DISTORTION

Receive path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
S_{TDRLS} (*)	Signal to Total Distortion (LSP-LSN) (up to 14dB attenuation) 8Ω Load Typical values are measured with 14dB attenuation.	Sinusoidal Test Method (measured using linear 300 Hz to 3400 Hz weighting, FS=8kHZ)				
		Level = +3 dBm0		77		dB
		Level = -6 dBm0	65	70		dB
		Level = -10 dBm0	62	67		dB
		Level = -20 dBm0	54	59		dB
		Level = -30 dBm0	44	49		dB
		Level = -40 dBm0	34	39		dB
		Level = -45 dBm0	29	34		dB
		Level = -55 dBm0	19	24		dB
	Signal to Total Distortion (LSP-LSN) (up to 14dB attenuation) 8Ω Load Typical values are measured with 14dB attenuation.	Sinusoidal Test Method (measured using linear 300 Hz to 6800 Hz weighting, FS=16kHZ)				
		Level = +3 dBm0		74		dB
		Level = -6 dBm0		67		dB
		Level = -10 dBm0		64		dB
		Level = -20 dBm0		56		dB
		Level = -30 dBm0		46		dB
		Level = -40 dBm0		36		dB
		Level = -45 dBm0		31		dB
		Level = -55 dBm0		21		dB
	Signal to Total Distortion (HPL, HPR) (up to 14dB attenuation) Typical values are measured with 14dB attenuation	Sinusoidal Test Method (measured using linear 300 Hz to 3400 Hz weighting, FS=8kHZ)				
		Level = +3 dBm0		74		
		Level = -6 dBm0		67		dB
		Level = -10 dBm0		64		dB
		Level = -20 dBm0		56		dB
		Level = -30 dBm0		46		dB
		Level = -40 dBm0		36		dB
		Level = -45 dBm0		31		dB
		Level = -55 dBm0		21		dB
	Signal to Total Distortion (HPL, HPR) (up to 14dB attenuation) Typical values are measured with 14dB attenuation	Sinusoidal Test Method (measured using linear 300 Hz to 6800 Hz weighting, FS=16kHZ)				
		Level = +3 dBm0		71		
		Level = -6 dBm0		64		dB
		Level = -10 dBm0		61		dB
		Level = -20 dBm0		53		dB
		Level = -30 dBm0		43		dB
		Level = -40 dBm0		33		dB
		Level = -45 dBm0		28		dB
		Level = -55 dBm0		17		dB

(*) The limit curve shall be determined by straight lines joining successive coordinates given in the table.

VOICE CODEC DISTORTION

Transmit path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
S_{TDX} (*)	Signal to Total Distortion (up to 35dB gain) FS frequency = 8kHz. Typical values are measured with 30.5dB gain	Sinusoidal Test Method (measured using linear 300 Hz to 3400 Hz weighting) FSS = 0				
		Level = +3 dBm0		75		dB
		Level = 0 dBm0	68	73		dB
		Level = -6 dBm0	64	68		dB
		Level = -10 dBm0	59	64		dB
		Level = -20 dBm0	49	54		dB
		Level = -30 dBm0	40	44		dB
		Level = -40 dBm0	30	34		dB
		Level = -45 dBm0	25	29		dB
		Level = -55 dBm0	15	19		dB
	Signal to Total Distortion FS frequency = 16kHz. Typical values are measured with 30.5dB gain	Sinusoidal Test Method (measured using linear 300 Hz to 6800 Hz weighting) FSS = 1				
		Level = +3 dBm0		72		dB
		Level = 0 dBm0		70		dB
		Level = -6 dBm0		65		dB
		Level = -10 dBm0		61		dB
		Level = -20 dBm0		51		dB
		Level = -30 dBm0		41		dB
		Level = -40 dBm0		31		dB
		Level = -45 dBm0		26		dB
		Level = -55 dBm0		16		dB

(*) The limit curve shall be determined by straight lines joining successive coordinates given in the table.

STEREO AUDIO DAC and FM CHARACTERISTICS

Unless otherwise specified, V_{CC} = 2.7V to 3.3V, T_{amb} = -30°C to 85°C; typical characteristics are specified at V_{CC} = 3V, VCMHP=1.5V, T_{amb} = 25°C; f_{AMCK} = 13.0MHz; Full-Scale Input Sine Waves at 1015.625Hz; Input Sample Rate (Fs) = 48kHz; Input Data = 18Bits; Measurement Bandwidth is 20Hz to 20kHz, unweighted. Resistive load on HPL, HPR = 16Ω).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
N	Resolution*				18	Bits
DYNR	Dynamic Range	A-weighted	89	93		dB
SNR	Signal to noise ratio	2Vpp output HPL, HPR gain set to -6dB 16Ω load A-weighted unweighted (20 Hz to 20 kHz)		 93 87		 dB dB
THDL	Total Harmonic Distortion Worst case load	$2V_{pp}$ output HPL, HPR gain set to -6dB 16Ω load		0.01	0.03	%
THD	Total Harmonic Distortion	$2V_{pp}$ output HPL, HPR gain set to -6dB 1kΩ load		0.004		%
	Deviation from Linear Phase*	Measurement Bandwidth 20Hz to 20kHz, Fs= 48kHz. Combined digital and analog filter characteristics.			1	Deg
f_{PB}	Passband*	Combined Digital and Analog filter characteristics.	0		0.45Fs	kHz
	Passband Ripple*	Combined Digital and Analog filter characteristics.			0.2	dB
f_{SB}	StopBand*	Combined Digital and Analog filter characteristics.	0.55Fs			kHz
	StopBand Attenuationv	Measurement Bandwidth up to 3.45Fs Combined Digital and Analog filter characteristics.	50			dB
TSF	Transient suppression filter cutoff frequency**		15		23	Hz
	Out Of Band Noise	Measurement Bandwidth 20kHz to 100kHz. Zero input signal		-90		dBr
t_{gd}	Group Delay*			0.4		ms
	Interchannel Isolation*	2Vpp output HPR, HPL unloaded HPR, HPL with 16Ω to VCMHP		 100 55		 dB dB
	Interchannel Gain Mismatch				0.2	dB
	Gain Error				0.5	dB
SUT	Startup Time from Power Up**		9.3		13.8	ms

* Valid for Audio interface input (Audio Mode).

Calculation of TSF and SUT: we define: $k = (f_{AMCK} / f_{DIV})$ where f_{AMCK} is the frequency of **AMCK** expressed in Hz and $f_{DIV} = 6144000 \cdot (AMCK\_DIV+2)$, where AMCK_DIV is the content of **CR18**, bits1-0. The approximate startup time is obtained dividing 10.6 ms by ***k***, and the transient suppression filter cutoff frequency is obtained multiplying 20Hz for ***k***

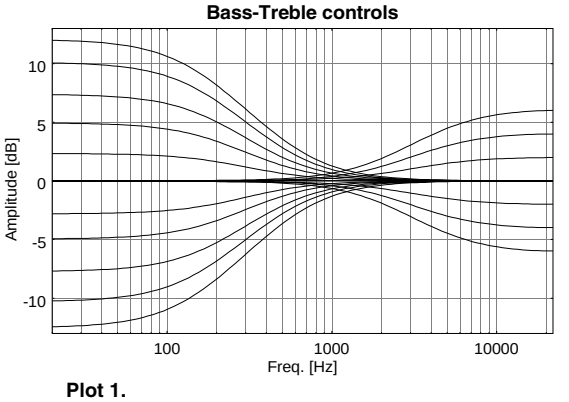
Note: Fs range: 8kHz - 48kHz.

POWER DISSIPATION

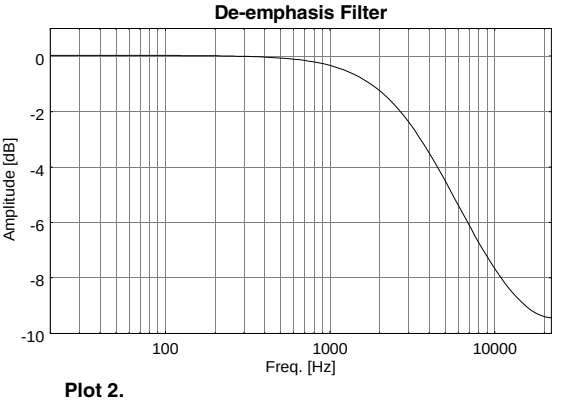
Unless otherwise specified, V_{CC} = 2.7V to 3.3V, T_{amb} = -30°C to 85°C, LSP, LSN and HPL, HPR outputs not loaded; typical characteristics are specified at V_{CC} = 3V, T_{amb} = 25°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC0}	Power down Current, REMOCON off	SDA, SCL= V_{CCIO}-0.1V REMOCON function disabled (REN = 0)		0.4		µA
I_{CC0R}	Power down Current, REMOCON on	SDA, SCL= V_{CCIO}-0.1V REMOCON function enabled (REN = 1) REMIN = V_{ILREM} or REMIN = V_{IHREM}		2		µA
I_{CC1}	Power Up Current in Voice Codec Mode	Fs=8kHz. LSP/N output selected		5	7	mA
I_{CC2}	Power Up Current in Stereo Audio Mode	Fs=44.1 kHz, AMCK=12 MHz HPL,HPR outputs selected, VCE=0, FSEL=0.		6	9	mA
I_{CC3}	Power Up Current in FM Stereo Mode	HPL,HPR outputs selected, VCE=0.		2	4	mA

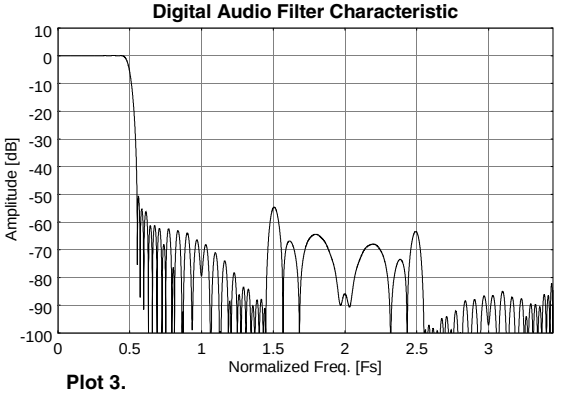
TYPICAL PERFORMANCE CHARACTERISTICS (simulations)



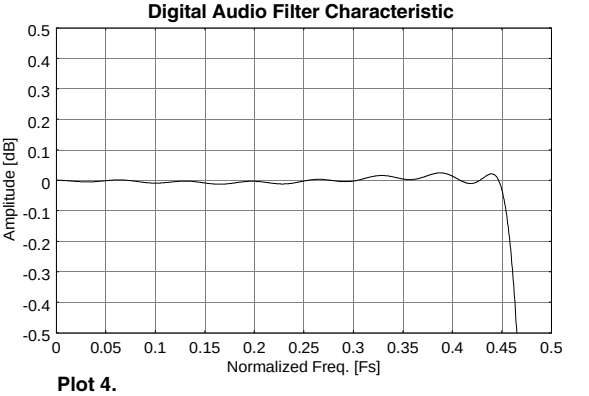
Plot 1.
Bass and treble gains are independently selectable in any combination. Filters characteristics at Fs=44.1kHz are plotted



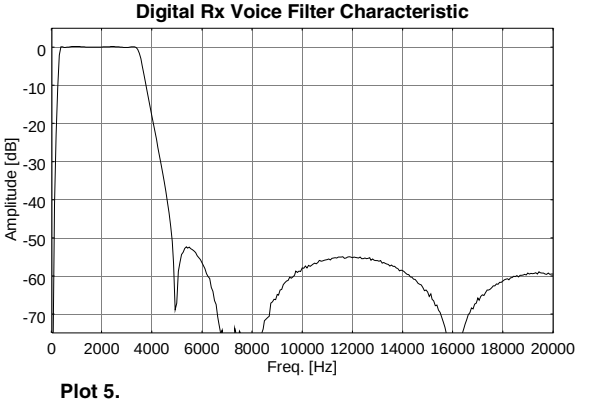
Plot 2.
The filter compensates for pre-emphasis used on some audio CDs. The gain error from ideal filtering is lower than 0.1dB. The de-emphasis filter selection implies a flat treble control.



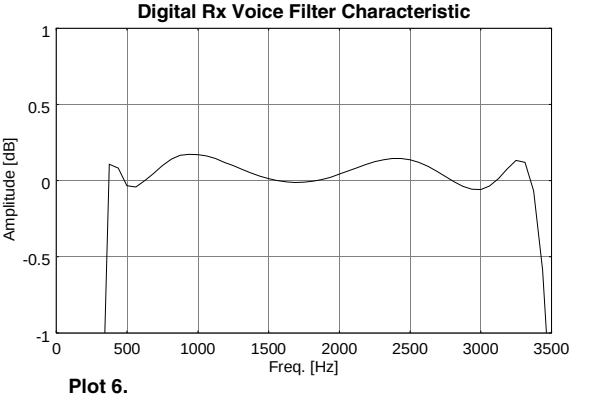
Plot 3.
Frequency response up to 3.45 Fs



Plot 4.
In band Frequency response

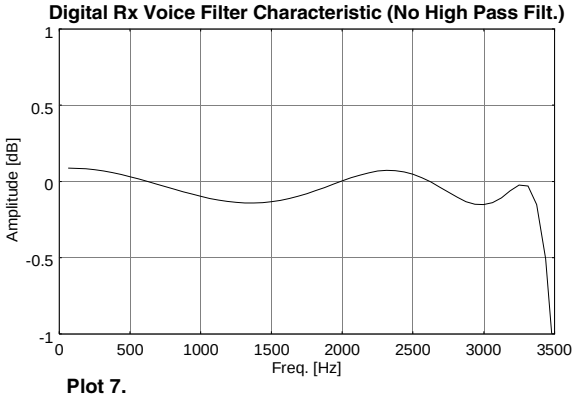


Plot 5.
Frequency response up to 2.5Fs

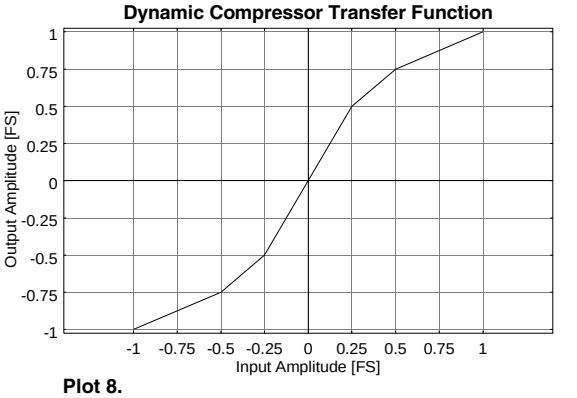


Plot 6.
In band Frequency response. FS=8 kHz

TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

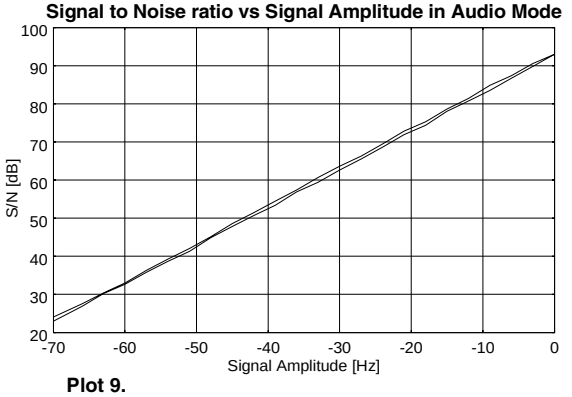


Plot 7.
In band Frequency response. FS=8 kHz
High Pass filter disabled (HPB=1).

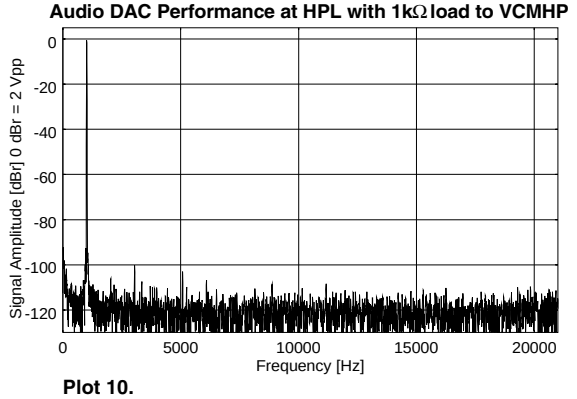


Plot 8.
Audio signal transfer function when the Dynamic Compressor is active.

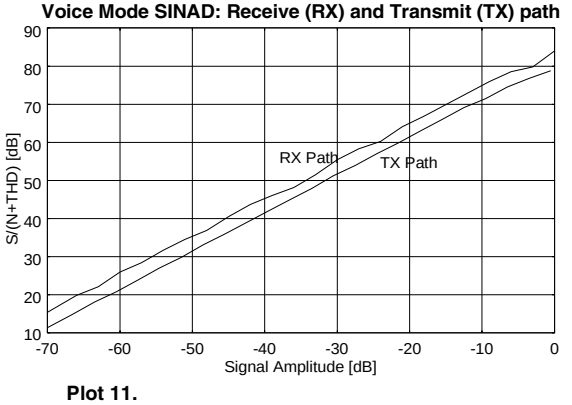
TYPICAL PERFORMANCE CHARACTERISTICS (Measures)



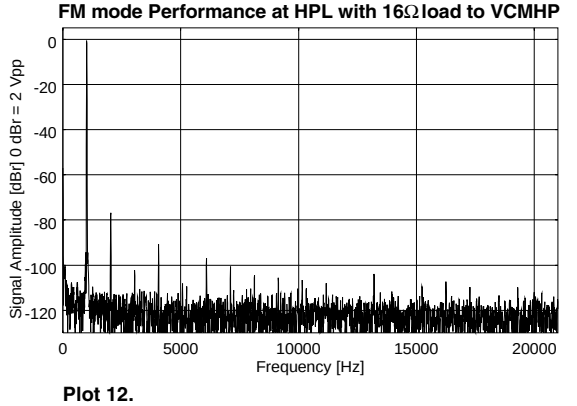
Plot 9.
1 kHz Input signal applied at Au I/ F input (L & R).
Left and right single ended drivers gain set to -6 dB.
VCC=2.7V, Fs=48kHz, 18 bits input word. A-weighted



Plot 10.
FFT audio mode (8192 points). 1kΩ load
Full scale 1kHz input signal applied at Au I/ F input.
Both channels active, Left channel plotted
VCC=2.7V, Fs=48kHz, 18 bits input. 12MHz AMCK

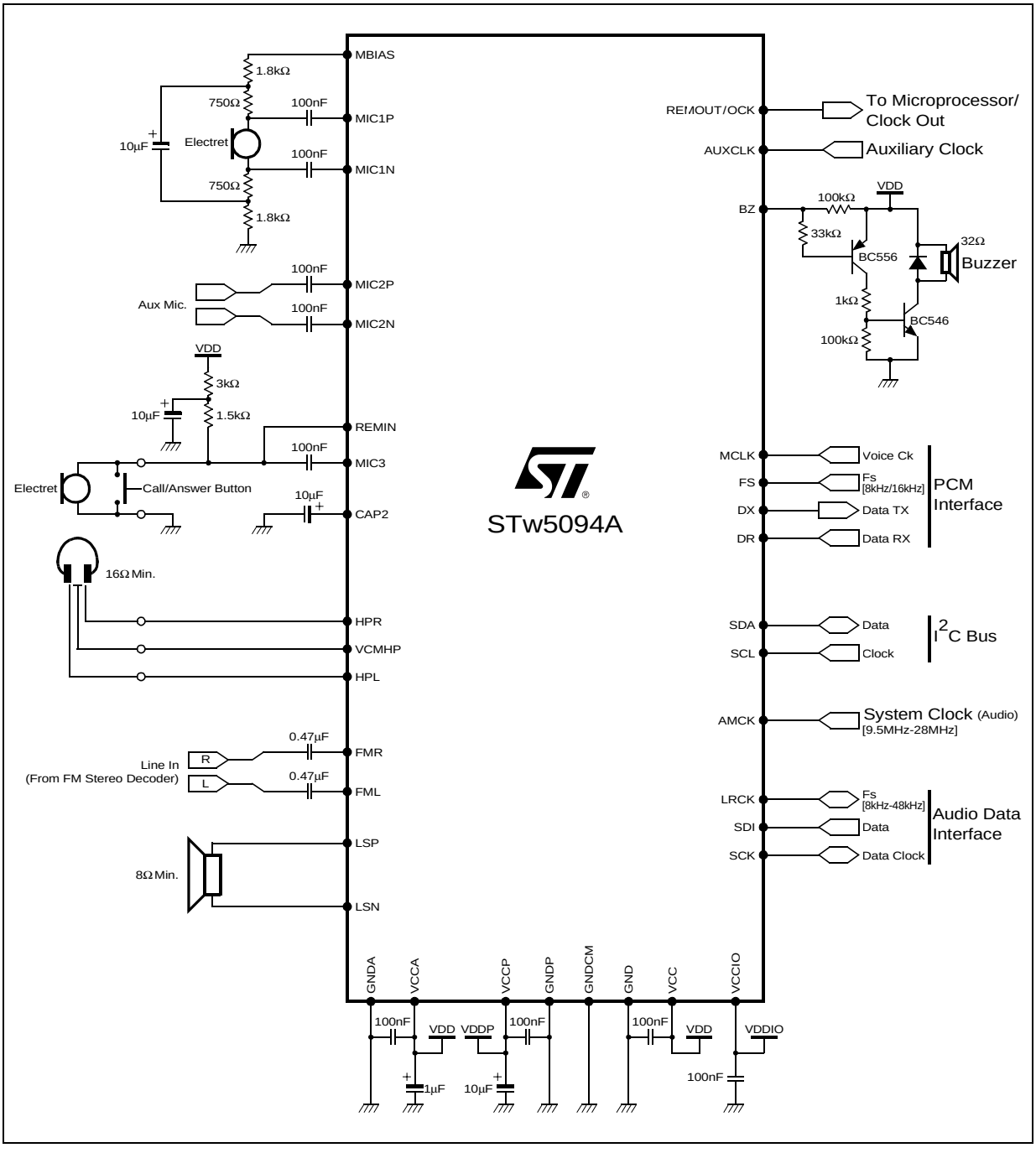


Plot 11.
1 kHz Signal applied at PCM (RX) or Mic1 (TX) input.
RX: 0 dB gain differential output (0dB=4Vpp out), 8Ω load.
TX: 20 dB input gain (0dB=0.2Vpp input).
VCC=2.7V, Fs=8kHz, 300-3400 Hz Linear Weight.



Plot 12.
FFT FM mode (8192 points). 16Ω load
1 kHz Signal applied at FM inputs
Both channels active and loaded, left channel plotted
VCC=2.7V, 12MHz AMCK

APPLICATION NOTE



TFBGA PACKAGE OUTLINE

Table 2. TFBGA 6x6x1.20 36 F6x6 0.80

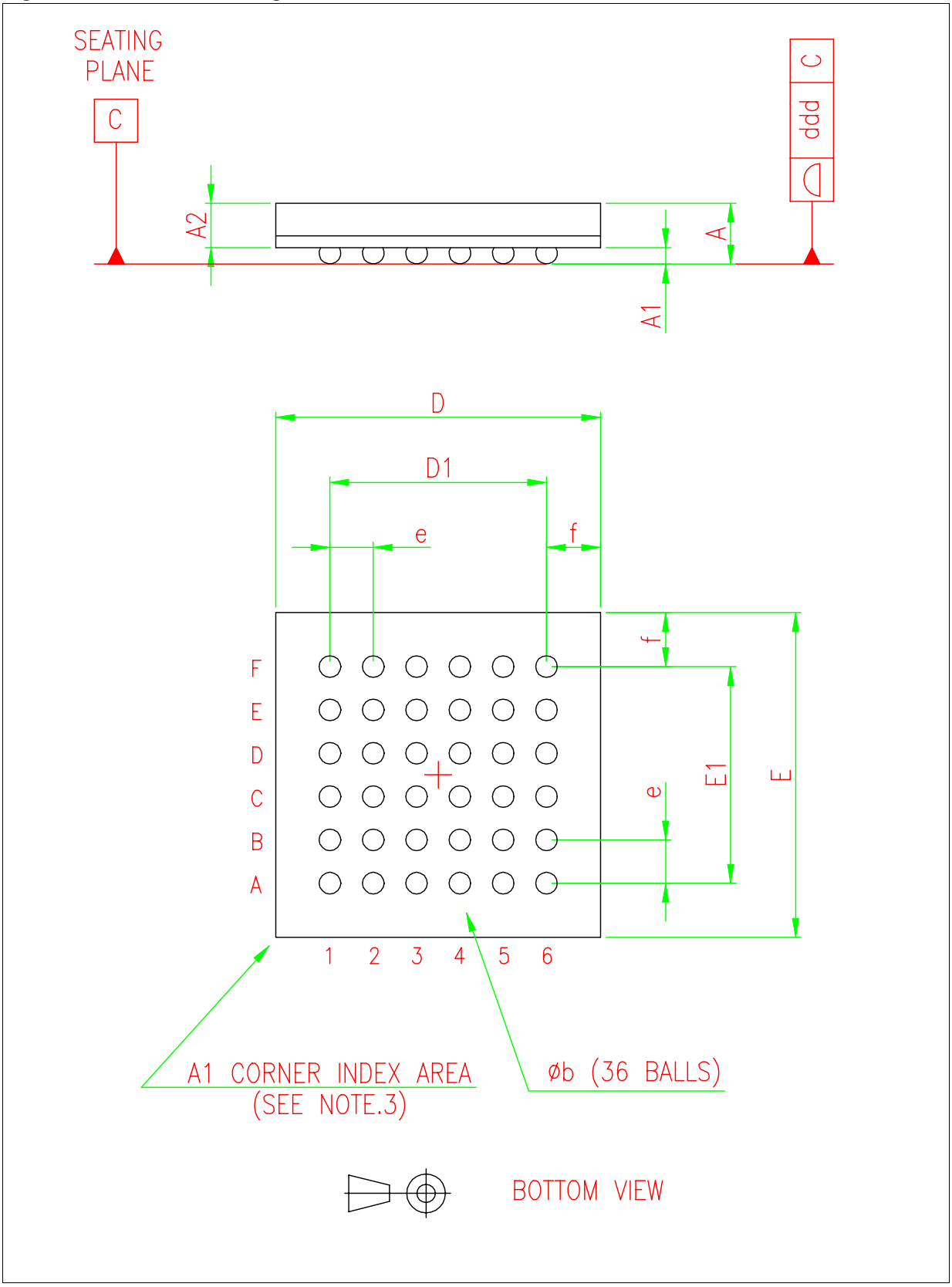
Ref	Min.	Typ.	Max.
A	1.01		1.20 (1)
A1	0.21		
A2		0.820	
b	0.35	0.40	0.45
D	5.85	6.00	6.15
D1		4.00	
E	5.85	6.00	6.15
E1		4.00	
e	0.72	0.80	0.88
f	0.85	1.00	1.15
ddd			1.00

1.Max mounted height is 1.16 mm. Based on a 0.37 mm ball pad diameter.
Solder paste is 0.15 mm thick with 0.37 mm diameter.

(2) TFBGA stands for **T**hin **P**rofile **F**ine Pitch **B**all **G**rid **A**rray.
Thin profile: The total profile height (DIm A) is measured from the seating plane to the top of the component.
A = 1.01 to 1.20 mm
Fine pitch < 1.00 mm pitch.

(3) The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink, metallized markings or other feature of package body or integral heatslug.
A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner.
Exact shape of each corner is optional.

Figure 17. TFBGA36 drawing



REVISION HISTORY

Date	Revision	Description of Changes
9-Dec-2005	2	Minor changes: Typo in table title 1. Corrections in register description: Register CR20 - Bit 7 = 1 - FM sum function enabled
28-Apr- 2005	1	First Release

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