2-line IPAD™, ultra low capacitance protection for high speed USB

Features

- Ultra low diode capacitance (1.2 pF max)
- Two data lines (D+ and D-) protected against 15 kV ESD
- Breakdown voltage $V_{BR} = 6.0$ V min
- Flip Chip 400 µm pitch, lead-free
- Very low leakage current
- Very small PCB area
- RoHS compliant

Benefits

- Minimized impact on rise and fall times for maximum data integrity
- Low PCB space occupation
- Higher reliability offered by monolithic integration

Complies with the following standards

- IEC 61000-4-2 level 4 on external pins:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G - Method 3015.7
  - 25 kV (Human body model)

Application

- High speed USB port in wireless handsets (up to 480 Mb/s according to USB 2.0 high speed specification)

Description

The USBULC6-2F3 is a monolithic, application specific discrete device dedicated to ESD protection of high speed interfaces.

Its ultra low line capacitance secures a high level of signal integrity without compromising the protection of downstream sensitive chips against the most stringently characterized ESD strikes.

TM: IPAD is a trademark of STMicroelectronics.
1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{PP}</td>
<td>ESD discharge IEC 61000-4-2, air discharge</td>
<td>15</td>
<td>kV</td>
</tr>
<tr>
<td></td>
<td>ESD discharge IEC 61000-4-2, contact discharge</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>P_{PP}</td>
<td>Peak pulse power dissipation (8/20 μs)</td>
<td>60</td>
<td>W</td>
</tr>
<tr>
<td>T_j</td>
<td>Maximum junction temperature</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>T_{op}</td>
<td>Operating temperature range</td>
<td>-30 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>T_{stg}</td>
<td>Storage temperature range</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Table 2. Electrical characteristics (T_{amb} = 25 °C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>V_{BR}</td>
<td>Breakdown voltage</td>
<td>I_R = 1 mA</td>
<td>6</td>
<td>9</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_{RM}</td>
<td>Leakage current @ V_{RM}</td>
<td>V_{RM} = 3 V</td>
<td>100</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{CL}</td>
<td>Clamping voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_d</td>
<td>Dynamic impedance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{PP}</td>
<td>Peak pulse current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>α_T</td>
<td>Voltage temperature coefficient</td>
<td>I_R = 1 mA</td>
<td>5</td>
<td>10^{-4}/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_F</td>
<td>Forward voltage drop</td>
<td>V_{LINE} = 0 V, V_{OSC} = 30 mV, F = 1 MHz</td>
<td>1.2</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**USBULC6-2F3 Characteristics**

Figure 3. Eye diagram, board only (according to USB high speed specification)

Figure 4. Eye diagram, board with USBULC6-2F3 (according to USB 2.0 high speed specification)

Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge)

Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge)

Figure 7. Junction capacitance versus frequency (typical values)

Figure 8. Analog crosstalk measurement
Figure 9. S21 (dB) attenuation measurement

Figure 10. Digital crosstalk

Figure 11. Relative variation of peak pulse power versus initial junction temperature

Figure 12. Peak pulse power versus exponential pulse duration
2 Application information

Figure 13. Clamping voltage versus peak pulse current (typical values, exponential waveform)

Figure 14. Relative variation of leakage current versus junction temperature (typical values)

Figure 15. Application diagram
3 Ordering information scheme

Figure 16. Ordering information scheme

USB protection
Ultra Low Capacitance
Breakdown voltage
6 = $V_{MIN}$
Number of lines
2 = 2 lines
Package
F = Flip Chip
3 = Lead-free, pitch = 400 µm, bump = 255 µm

4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 17. Package dimensions
Figure 18. Footprint recommendations  Figure 19. Marking

Copper pad Diameter: 260 µm maximum
Solder mask opening: 300 µm minimum
Solder stencil opening: 220 µm recommended

Dot xx = marking
z = manufacturing location
yyw = datacode
(y = year
ww = week)

XXZ
YWW

User direction of unreeling

Note: More information is available in the application notes:
AN2348: “400 µm Flip Chip: Package description and recommendations for use”
AN1751: “EMI Filters: Recommendations and measurements”

5 Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Order code</th>
<th>Marking</th>
<th>Package</th>
<th>Weight</th>
<th>Base qty</th>
<th>Delivery mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>USBULC6-2F3</td>
<td>EH</td>
<td>Flip Chip</td>
<td>1.16 mg</td>
<td>5000</td>
<td>Tape and reel (7”)</td>
</tr>
</tbody>
</table>
# Revision history

Table 4. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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<tbody>
<tr>
<td>15-Dec-2006</td>
<td>1</td>
<td>Initial release.</td>
</tr>
<tr>
<td>29-Apr-2008</td>
<td>2</td>
<td>Updated ECOPACK statement. Updated <em>Figure 17</em>, <em>Figure 18</em> and <em>Figure 20</em>. Reformatted to current standards.</td>
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